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Advisor: Paolo Bernardi
Ph.D. in Computer and Control Engineering
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New Techniques for Reliability Characterization of Electronic Circuits
Reliability
Reliability

The ability of a system or component to perform its required functions under stated conditions for a specified period of time.” (IEEE Glossary)
The Bathtub Curve

Cradle to grave instantaneous failure rate vs. time

- Infant Mortality
  - Decreasing Failure Rate

- Normal Life (Useful Life)
  - Low "Constant" Failure Rate

- End of Life Wear-Out
  - Increasing Failure Rate
The Bathtub Curve

Cradle to grave instantaneous failure rate vs. time

Increased Failure Rate

Infant Mortality
Decreasing Failure Rate

End of Life Wear-Out
Increasing Failure Rate

Normal Life (Useful Life)
Low "Constant" Failure Rate

Time

Failures causes in "Normal life"

radiation
Failures causes in "Normal life"

- radiation
- $\alpha$ rays
- high-energy particles

- environment
- temperature
- humidity

- maximum ratings
- voltage
- current density

- contamination
- gas
- dust

- magnetic and electrical fields.

- mechanical stress
- vibration
- shock
- pressure
New Techniq Characterization
How do we characterize? → Testing

apply specific signals to the inputs (test patterns or test vectors) → measure the output responses → compare them with known good response (golden solution)

GO ↔ no GO

diagnosis

pass/fail test
Manufacturing testing

- Wafer sorting
- ATE
- After packaging testing
- Burn in

Online testing

- Periodic testing
- On demand testing
Tests for Reliability of Electronic Circuits
System-on-a-Chip

Microprocessors

Memories

MEMS Sensors

Analog-to-digital Converters
Microprocessors testing issues

- fault coverage (%)
- at (maximum) speed
- diagnostic information
- standard test access mechanisms
- area (or memory) overhead
- acceptable total test time
- Intellectual Property
- respect power consumption constraints
- respect online timing constraints
- transparent execution w.r.t.
- system state
- data memory content
- dependant on system configuration
- faulty execution may lead to hazardous condition
Software-Based Self-Test

SBST test program

Code memory

Data memory

Test results

μP

Code

address/ctrl

system bus

data

code
New Techniques in Characterization of Enzymes
Microprocessors Hardware Self-Test
MIHST

- Compact test program
- Test results

Diagram showing the interactions between code memory, data memory, MUX, and CPU in a self-test scenario.
Encoding Method

Original Program

XOR R3, R3
MOV R2, #0
loop: ADD R3, R3, R2
INC R2
CMP R2, K
JNE loop
MOV [addr], R3
...

Hidden operands update

XOR R3, R3
MOV R2, #0
loop: ADD R3, R3, #0 (+1)
CMP R2, K
JNE loop
MOV [addr], R3
...

Autonomous flow control

XOR R3, R3
(do K times) ADD R3, R3, #0 (+1)
MOV [addr], R3
...

Encoding format

Example
Encoding format

OPCode word

size(OPC)  n  n

opcode  iloop  oloop

OPERand word(s)

size(imm)  m  1

operand seed  manip  rst
Original Program

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operand seed  manip  rst

Example

OPCode

opcode  iloop  oloop

ADD  K  1

OPErand

operand seed  manip  rst

1  R3  -
2  R3  -
3  0  inc  1
Disassociation of addresses

Program code

<table>
<thead>
<tr>
<th>Address</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:</td>
<td>MOV R2, #2</td>
</tr>
<tr>
<td>2:</td>
<td>loop: DEC R2</td>
</tr>
<tr>
<td>3:</td>
<td>JNZ dest1</td>
</tr>
<tr>
<td>4:</td>
<td>JP dest2</td>
</tr>
<tr>
<td>5:</td>
<td>MOV, R3, #0</td>
</tr>
<tr>
<td>6:</td>
<td>dest1: ADD R3, R3, R2</td>
</tr>
<tr>
<td>7:</td>
<td>JP loop</td>
</tr>
<tr>
<td>Y:</td>
<td>dest2: MOV, R3, #0</td>
</tr>
</tbody>
</table>

1: MOV R2, #2
2: DEC R2
3: JNZ dest1
6: ADD R3, R3, R2
7: JP loop
Y: MOV, R3, #0
Y+1: ADD R3, R3, R2
Y+2: JP loop
2: ...

executed from memory

executed from MIHST
Microprocessors Hardware Self-Test

MIHST
MIHST on-line procedure

0. START The on-line test interrupt signal is activated
1. The microprocessor unit saves the system context.
2. The system control is given to the ISR, which:
   • stores all the GPRs the test program uses,
   • activates the test_mode signal (enables the MIHST module).
3. Control is given to the MIHST module, which:
   • cleans the pipeline (NOPs),
   • reproduces the compacted test program,
   • aligns the pipeline (NOPs),
   • generates a “jump N” instruction for the CPU,
   • resets the test_mode signal and disables the MIHST module.
4. Control is given back to the ISR, which:
   • restores the GPR contents,
   • executes the Return From Interrupt instruction.
5. END The microprocessor restores the system context and resumes its latter task.
Case Study

miniMIPS processor
• 5 stages
• 32-bit data bus
• 32-bit address bus
• 22,208 cells

MIHST unit
• 28 bits OPCode words
• 23 bits register OPERand words
• 7 bits immediate OPERand words
• 72-bit MISR module
• 3,590 cells
Overall miniMIPS testing results

Case Study

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<table>
<thead>
<tr>
<th></th>
<th>Test time (clock cycles)</th>
<th>Program size (bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBST</td>
<td>34,233</td>
<td>10,344</td>
</tr>
<tr>
<td>MIHST</td>
<td>4,200</td>
<td>400</td>
</tr>
</tbody>
</table>
Advantages of the MIHST module

- Defect coverage
- Speed
- Confidentiality
- Robustness
- Modularity
- Ease of integration
- Limited intrusiveness
- Programmability
- Scalability
- Low cost
Publications & Conference participation

SETS
ITC

2010

3D-TEST (ITC)
DDEC5
ETS
IDT

Journal - ToIM

2011

IOLTS
Journal - JETTA

2012

SETS
SDD

Publication Chair
SBST for pipelined microprocessors: BTB, PI&RF and address adder unit
Embedded memories diagnosis testing platform

MIHST architecture for online testing

MIHST-based microprocessor testing

FPGA assisted parallel testing platform

MIHST-based embedded memories testing

2013

ITC (submitted)
Journal - ToC (major revision)
Collaboration with national and international industries and entities
Training and teaching activities

36 credits
Politecnico di Torino (Politecnico di Torino) 3rd level and "high qualification" courses

9 credits
Regional project "Banda di Alta Formazione"

10 credits
- IEEE TSS Spring school
- Vienna University of Technology Summer school

Tutorials
2 full-day IEEE tutorials
2 half-day IEEE tutorials

55 credits
Training
Teaching

80 hours lab. sessions
advisor in master thesis
Conclusions

I participate actively in the international community and in internal PoliTO activities.

I developed innovative reliability characterization techniques for electronic circuits (microprocessors, memories, MEMS sensors, mixed signal devices); both for manufacturing and online testing.

All the knowledge acquired and generated during these years has been published in several international, peer-reviewed journals and conference proceedings.
Thank you!

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