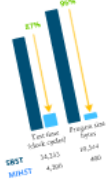


Overall miniMIPS testing results

Case Study

- miniMIPS processor**
- 32-bit
 - 32-bit data bus
 - 32-bit address bus
 - 32-bit cache
- MIHST work**
- 32 bits CPU cache
 - 32 bits register file
 - 7 bits address bus
 - 7 bits data bus
 - 32-bit cache
 - 32-bit cache



Advantages of the MIHST module

- Defect coverage
- Speed
- Confidentiality
- Robustness
- Modularity
- Ease of integration
- Limited intrusiveness
- Programmability
- Scalability
- Low cost



Publications & Conference participation



Collaboration with national and International Industries and entities



Training and teaching activities



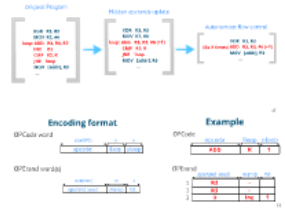
Conclusions

Proposes activity to the microelectronics and electrical PNTD activities. Developed a novel and efficient design methodology for the electronic circuits design, especially, in the VLSI systems (in digital domain), both for microelectronics and other systems.

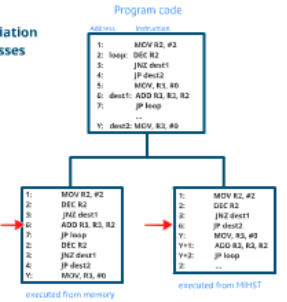
All the knowledge acquired and generated during these years has been published in several international, peer-reviewed journals and conference proceedings.



Encoding Method



Disassociation of addresses



memory is almost 50-60% of SoCs area

Thank you!

Lil' M. Cigada Boica
 Address: Paula Bernard
 Ph.D. in Computer and Control Engineering
 March 2013



New Techniques for Reliability Characterization of Electronic Circuits



Microprocessors testing issues

- High coverage TDD
- Full coverage TDD
- Augmented information
- Enabled from system architecture
- Able to measure coverage
- Able to measure coverage
- Independent on system configuration
- Scalability: from 100k to 1M
- Fully reconfigurable and testable
- Functional Integrity
- Reduced power or memory block constraints
- Support cellular, SWaP, cloud data
- Supports memories (e.g., 1-10MB SRAM)
- Supports on-chip configuration
- Supports on-chip configuration
- Supports on-chip configuration
- Supports on-chip configuration
- Supports on-chip configuration

Lyl M. Ciganda Brasca

Advisor: Paolo Bernardi

Ph.D. in Computer and Control Engineering

March 2013



Four thick, teal-colored curved lines are positioned around the central text, pointing towards it from the top-left, top-right, bottom-left, and bottom-right corners.

New Techniques for Reliability Characterization of Electronic Circuits



Reliability

Electronic Circuits

Reliability

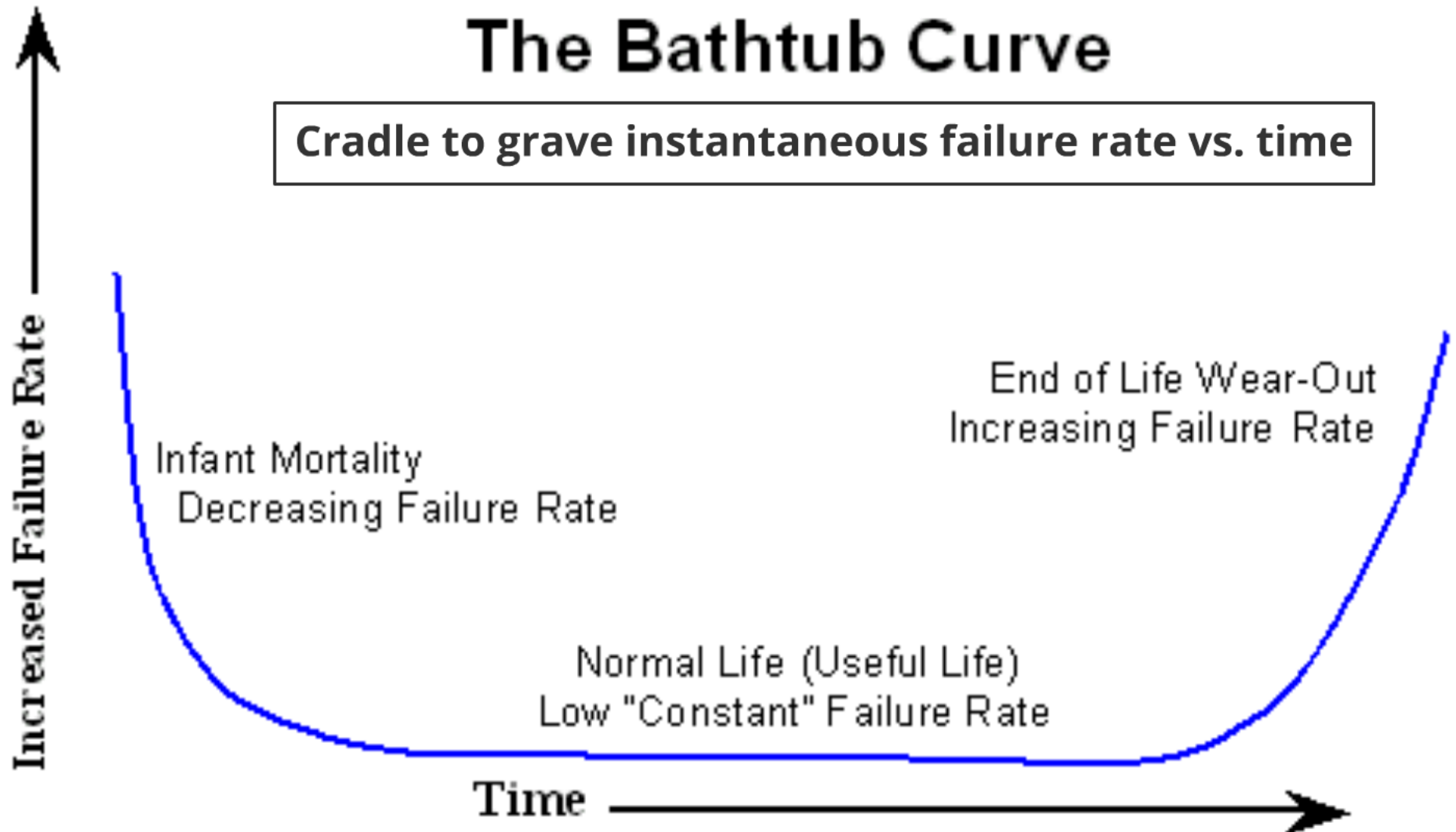


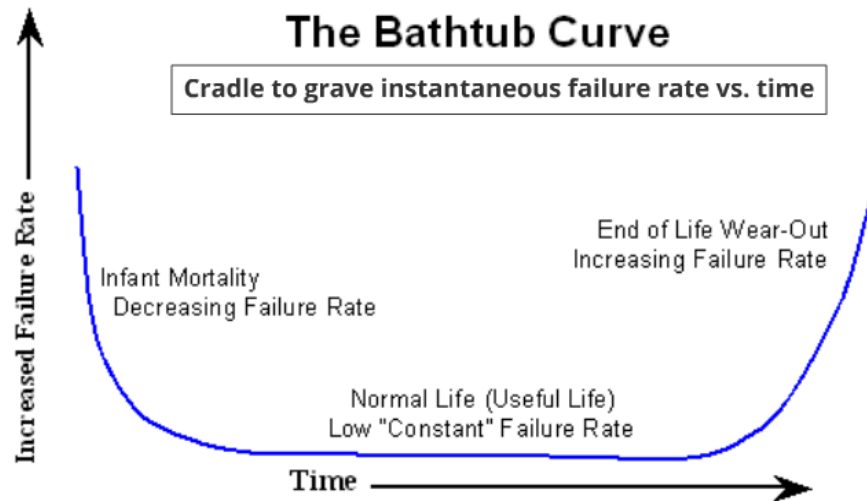
The ability of a system or component to perform its required functions under stated conditions for a specified period of time.”

(IEEE Glossary)

The Bathtub Curve

Cradle to grave instantaneous failure rate vs. time





4



5

Failures causes in "Normal life"

radiation

Failures causes in "Normal life"

radiation

α rays

high-energy particles

contamination

gas

dust

environment

temperature

humidity



magnetic and
electrical **fields.**

maximum ratings

voltage

current density

mechanical stress

vibration

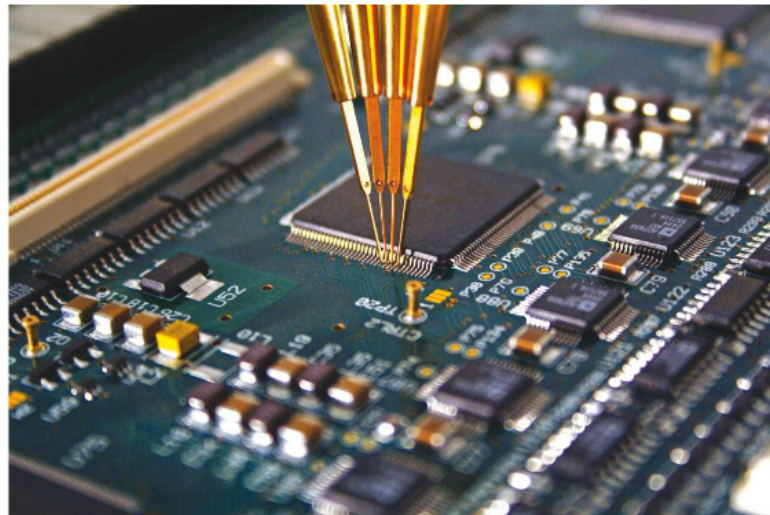
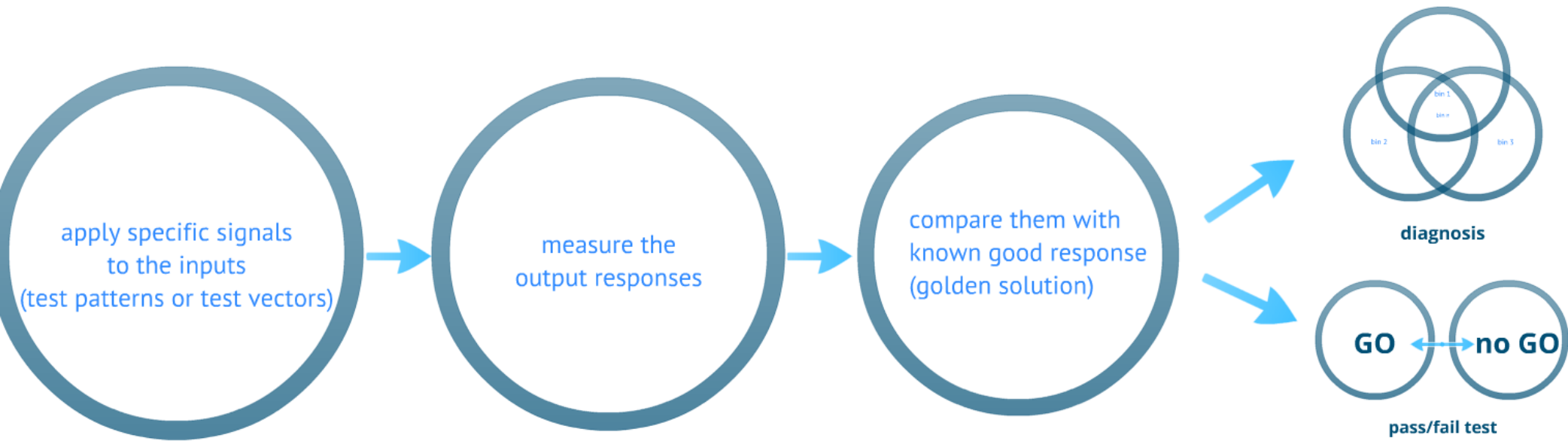
shock

pressure

New Techniques Characterization

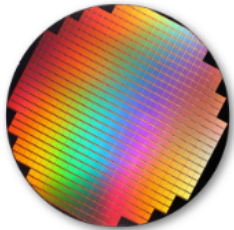


How do we characterize? → Testing

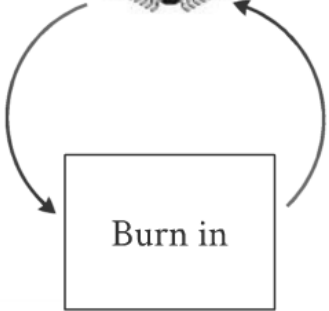


Manufacturing testing

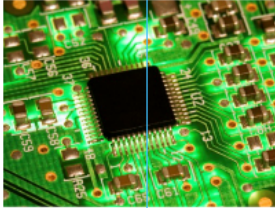
Wafer sorting



After packaging testing

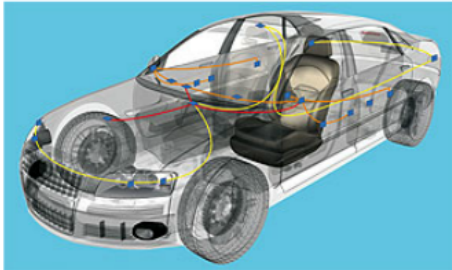


ATE



Online testing

Periodic testing

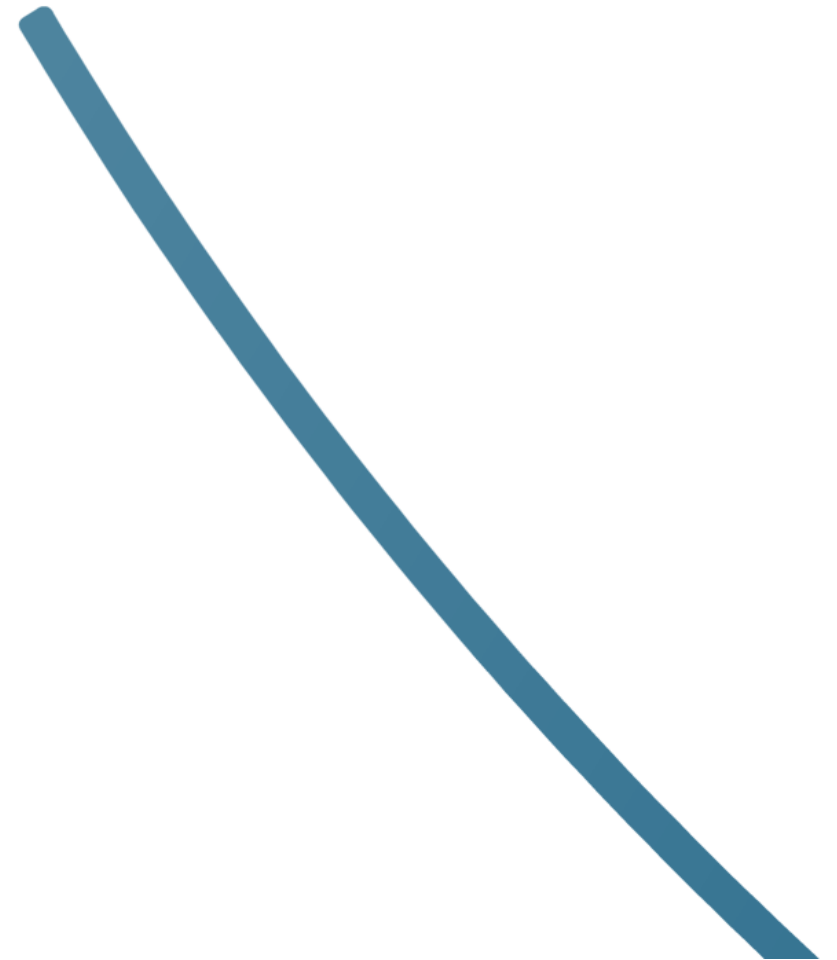


On demand testing



s for Reliability

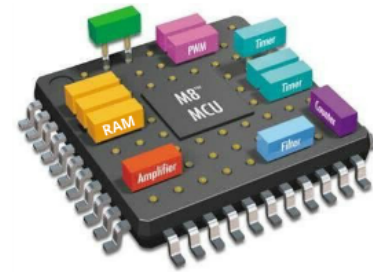
Electronic Circuits



System-on-a-Chip

Microprocessors

Memories



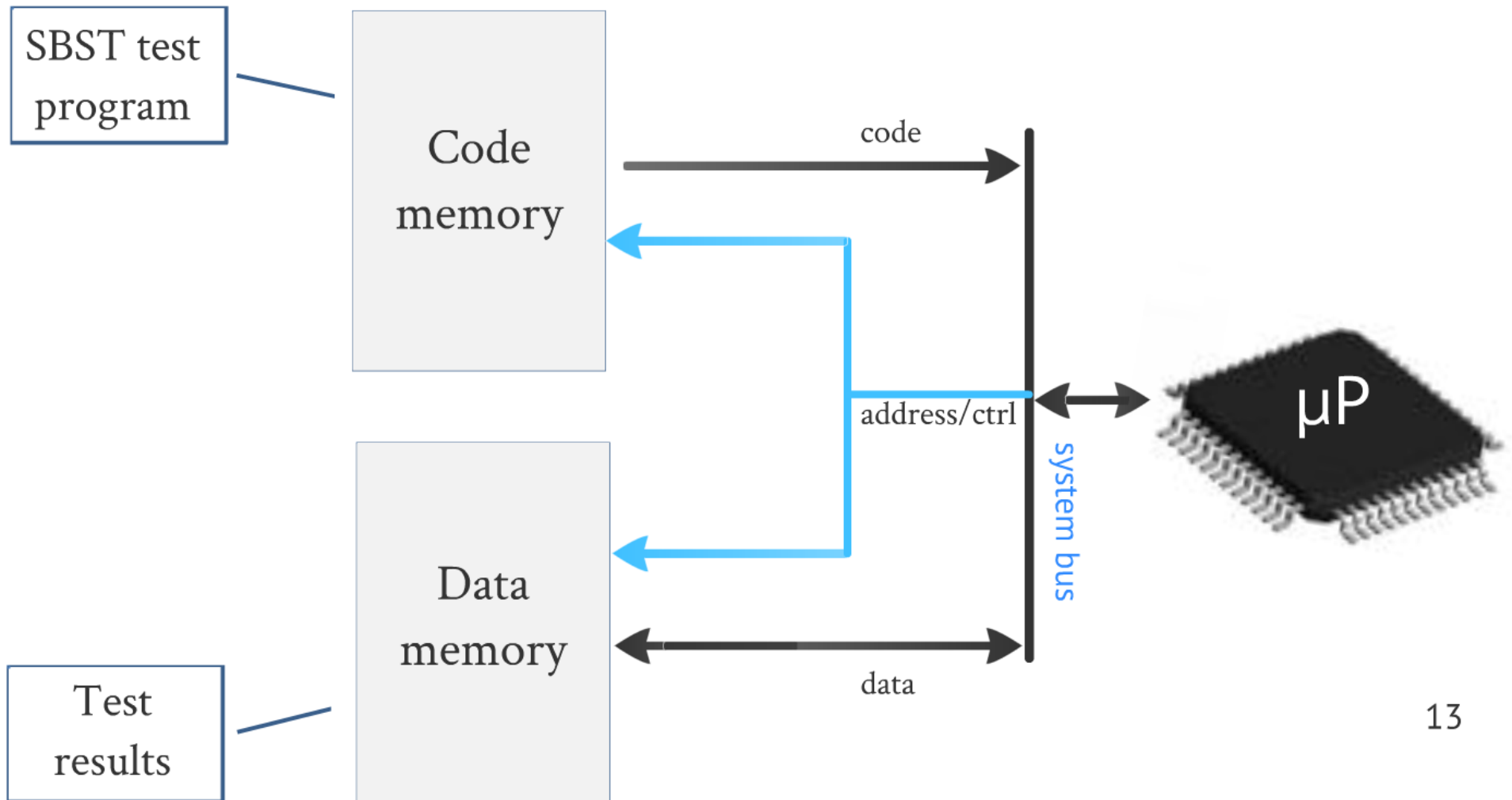
MEMS Sensors

Analog-to-digital Converters

Microprocessors testing issues

- fault coverage (%)
- at (maximum) speed
- diagnostic information
- standard test access mechanisms
- area (or memory) overhead
- acceptable total test time
- Intellectual Property
- respect power consumption constraints
- respect online timing constraints
- transparent execution w.r.t.
 - system state
 - data memory content
 - dependant on system configuration
- faulty execution may lead to hazardous condition

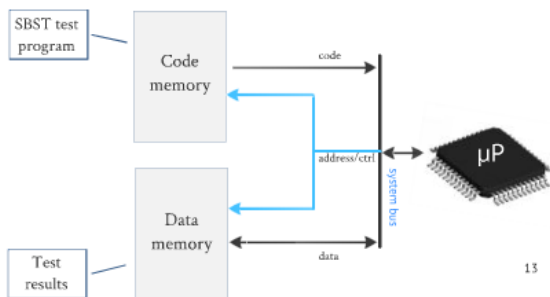
Software-Based Self-Test





Microprocessors testing issues

Software-Based Self-Test



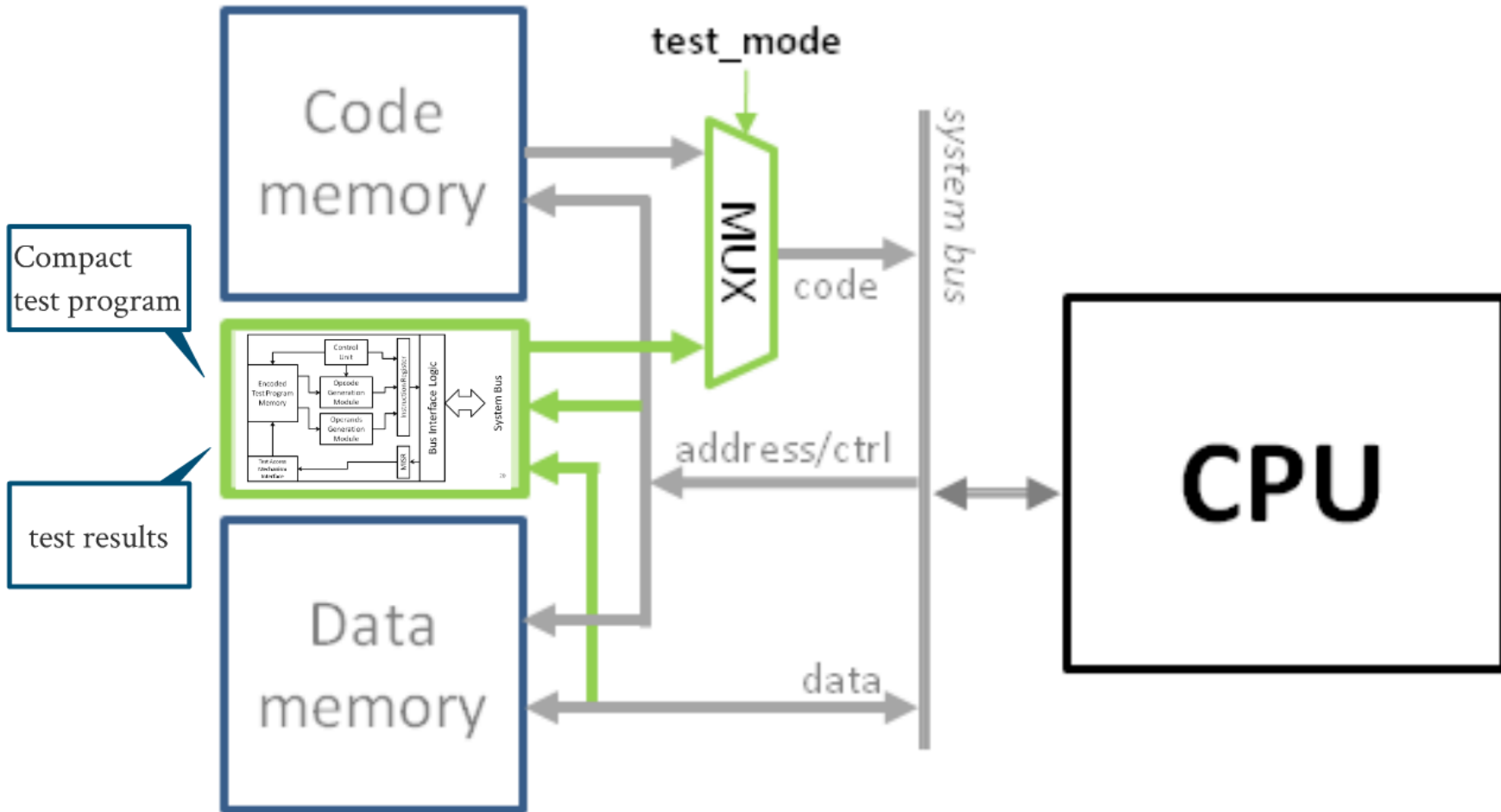
13

- fault coverage (%)
- at (maximum) speed
- diagnostic information
- standard test access mechanisms
- area (or memory) overhead
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- respect power consumption constraints
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 - system state
 - data memory content
 - dependant on system configuration
 - faulty execution may lead to hazardous condition



New Techniques Characterization of E

Microprocessors Hardware Self-Test MIHST



Encoding Method

Original Program

```
XOR R3, R3
MOV R2, #0
loop: ADD R3, R3, R2
INC R2
CMP R2, K
JNE loop
MOV [addr], R3
...
```

Hidden operands update

```
XOR R3, R3
MOV R2, #0
loop: ADD R3, R3, #0 (+1)
CMP R2, K
JNE loop
MOV [addr], R3
...
```

Autonomous flow control

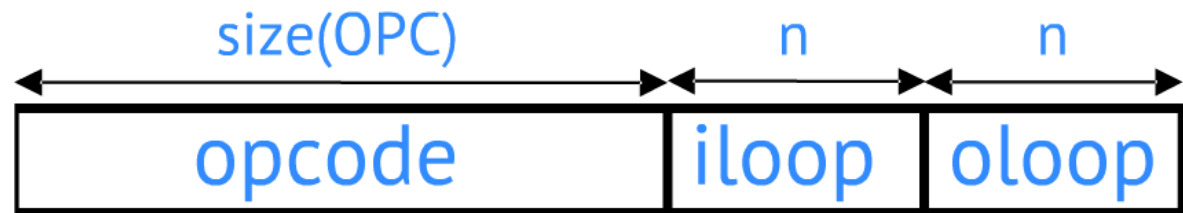
```
XOR R3, R3
(do K times) ADD R3, R3, #0 (+1)
MOV [addr], R3
...
```

Encoding format

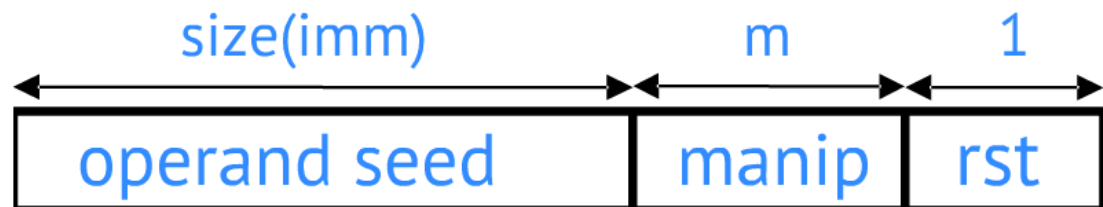
Example

Encoding format

OPCode word



OPERand word(s)



Original Program

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XOR R3, R3
MOV R2, #0
loop: ADD R3, R3, R2
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Autonomous flow control

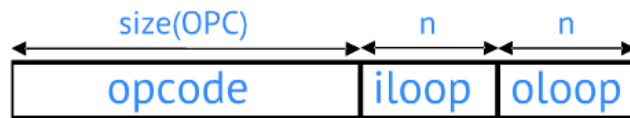
```

XOR R3, R3
(do K times) ADD R3, R3, #0 (+1)
MOV [addr], R3
...
    
```

17

Encoding format

OPCode word

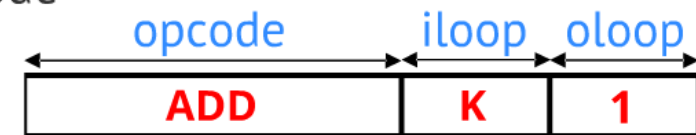


OPERand word(s)



Example

OPCode



OPERand


	operand seed	manip	rst
1	R3	-	
2	R3	-	
3	0	inc	1

19

Disassociation of addresses


Program code

Address	Instruction
1:	MOV R2, #2
2: loop:	DEC R2
3:	JNZ dest1
4:	JP dest2
5:	MOV, R3, #0
6: dest1:	ADD R3, R3, R2
7:	JP loop
	...
Y: dest2:	MOV, R3, #0



1:	MOV R2, #2
2:	DEC R2
3:	JNZ dest1
6:	ADD R3, R3, R2
7:	JP loop
2:	DEC R2
3:	JNZ dest1
4:	JP dest2
Y:	MOV, R3, #0

executed from memory

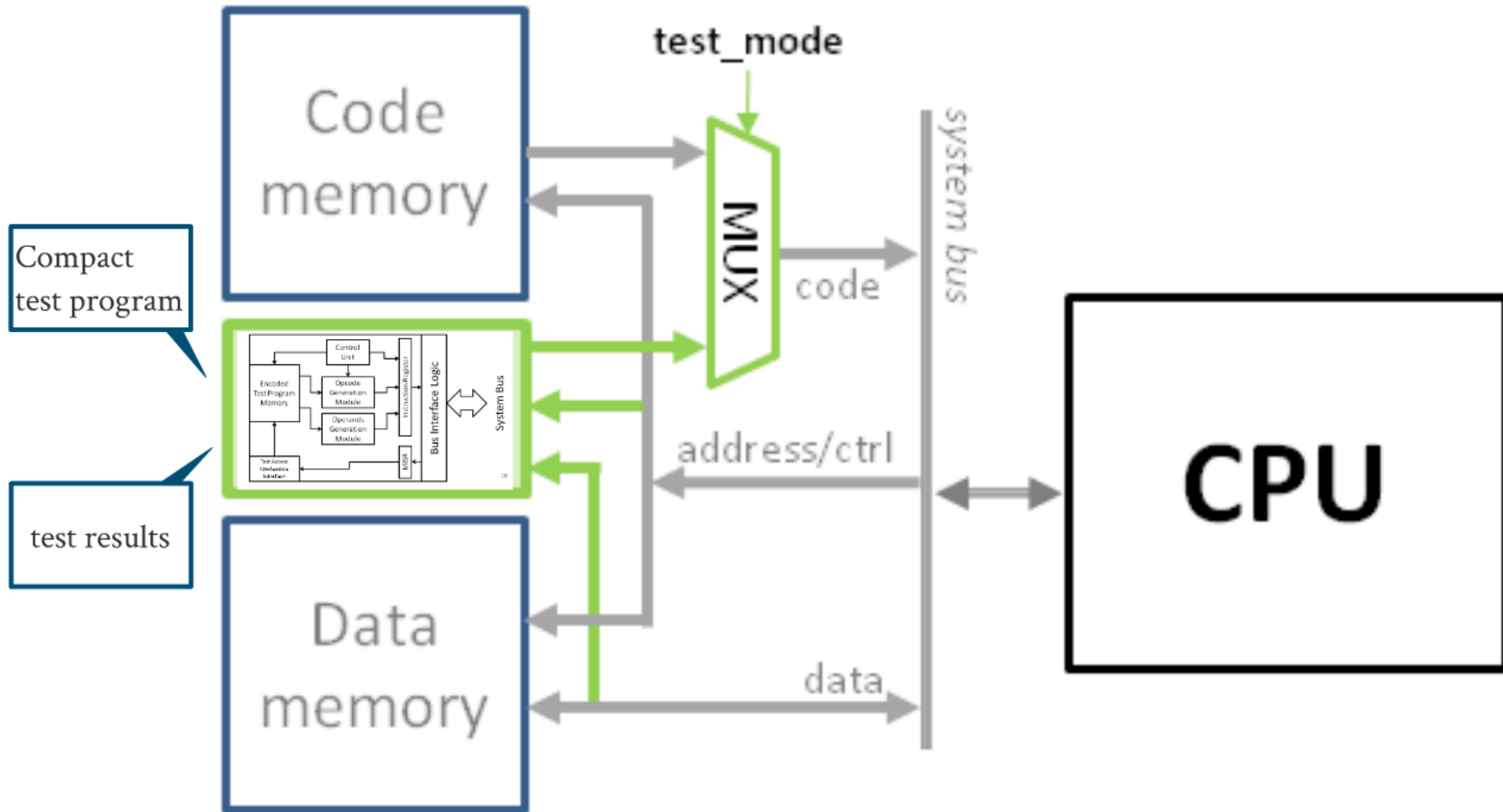


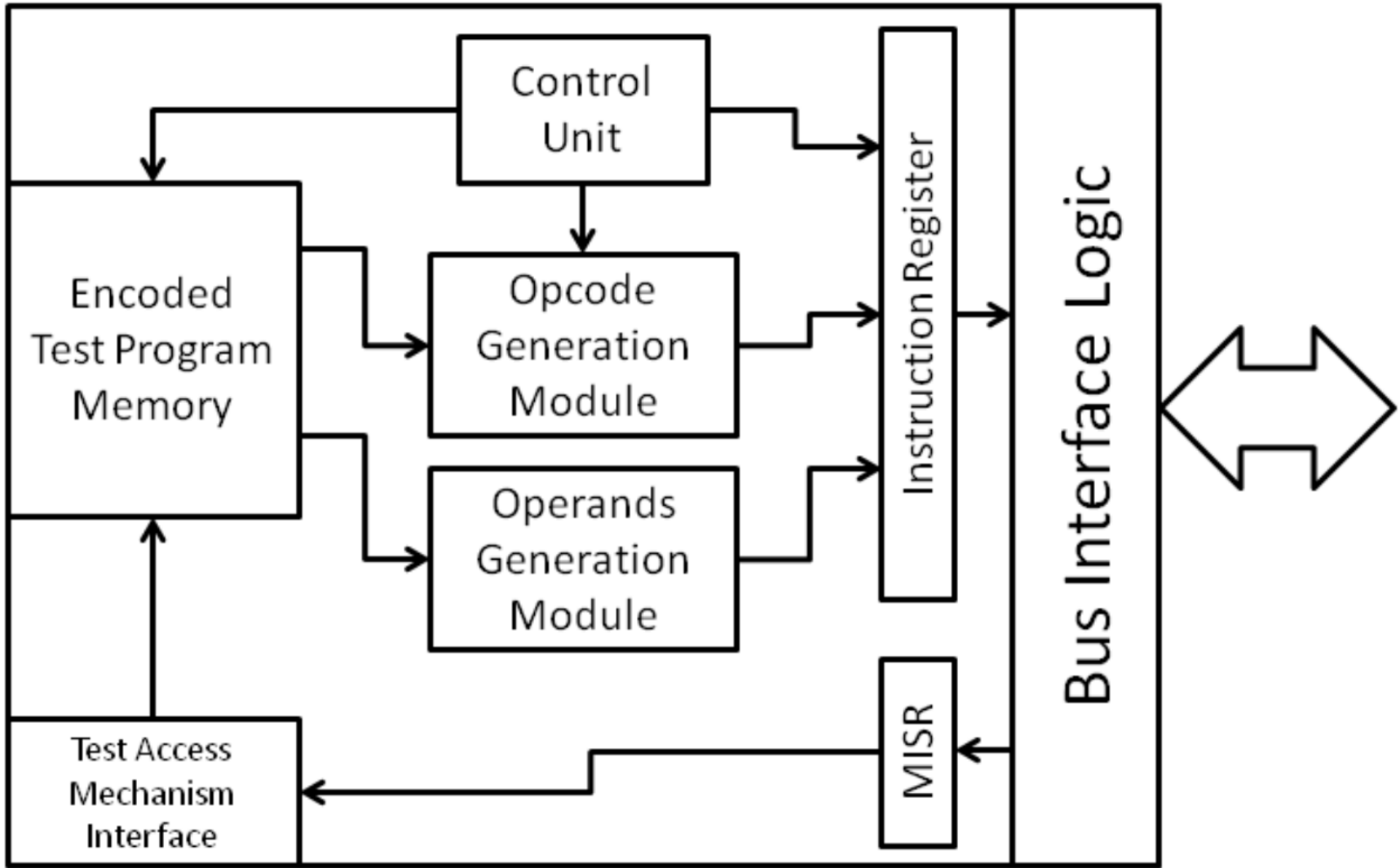
1:	MOV R2, #2
2:	DEC R2
3:	JNZ dest1
6:	JP dest2
Y:	MOV, R3, #0
Y+1:	ADD R3, R3, R2
Y+2:	JP loop
2:	...

executed from MIHST

Microprocessors Hardware Self-Test

MIHST

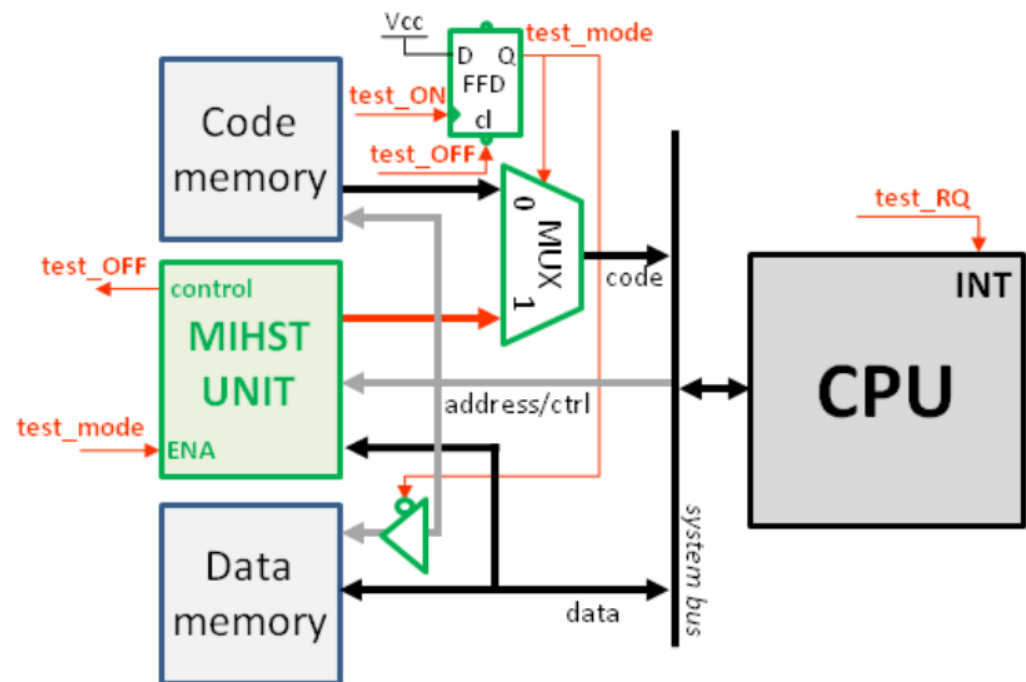




System Bus

MIHST on-line procedure

- 0 START The on-line test interrupt signal is activated
- 1 • The microprocessor unit saves the system context .
- 2 • The system control is given to the ISR, which:
 - stores all the GPRs the test program uses,
 - activates the test_mode signal (enables the MIHST module).
- 3 • Control is given to the MIHST module, which:
 - cleans the pipeline (NOPs),
 - reproduces the compacted test program,
 - aligns the pipeline (NOPs),
 - generates a “jump N” instruction for the CPU,
 - resets the test_mode signal and disables the MIHST module.
- 4 • Control is given back to the ISR, which:
 - restores the GPR contents,
 - executes the Return From Interrupt instruction.
- 5 END The microprocessor restores the system context and resumes its latter task.



Case Study

miniMIPS processor

- 5 stages
- 32-bit data bus
- 32-bit address bus
- 22,208 cells

MIHST unit

- 28 bits OPCode words
- 23 bits register OPErand words
- 7 bits immediate OPErand words
- 72-bit MISR module
- 3,590 cells

Overall miniMIPS testing results

Case Study

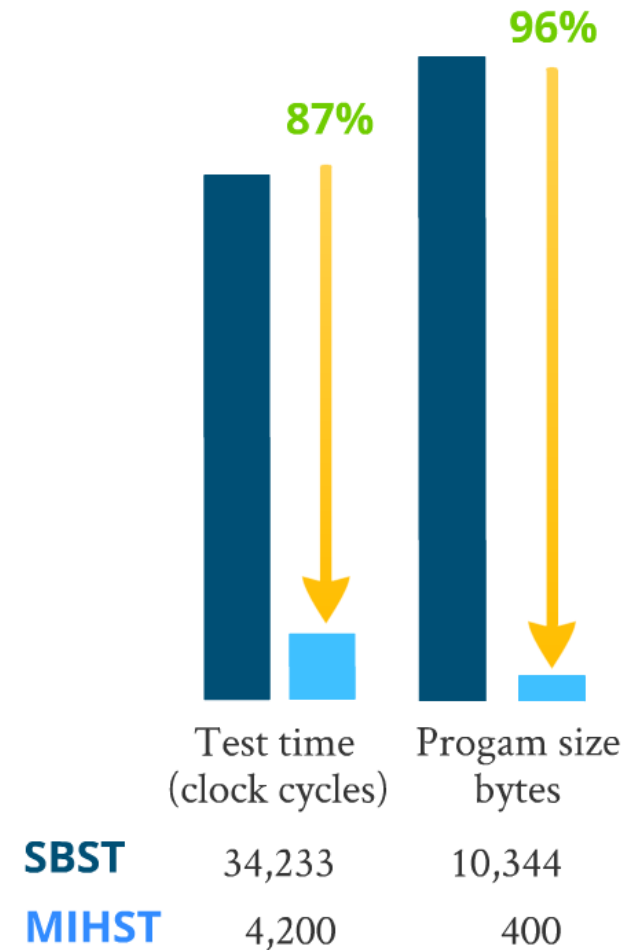
miniMIPS processor

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MIHST unit

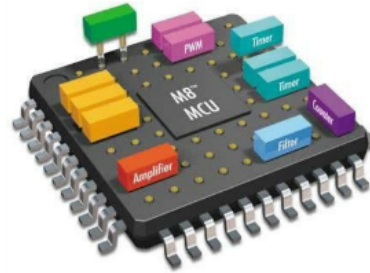
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22

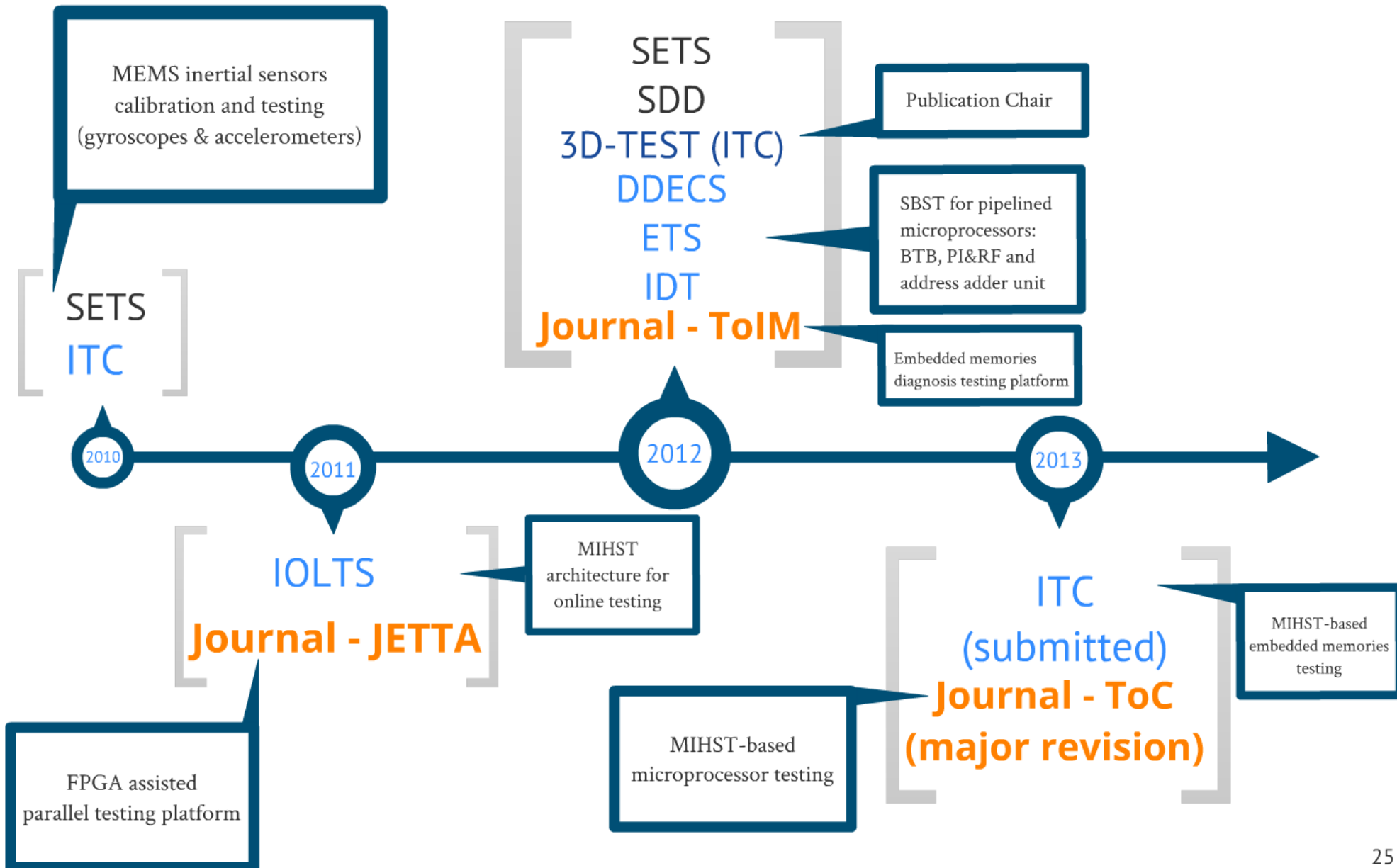


Advantages of the MIHST module

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- Confidentiality
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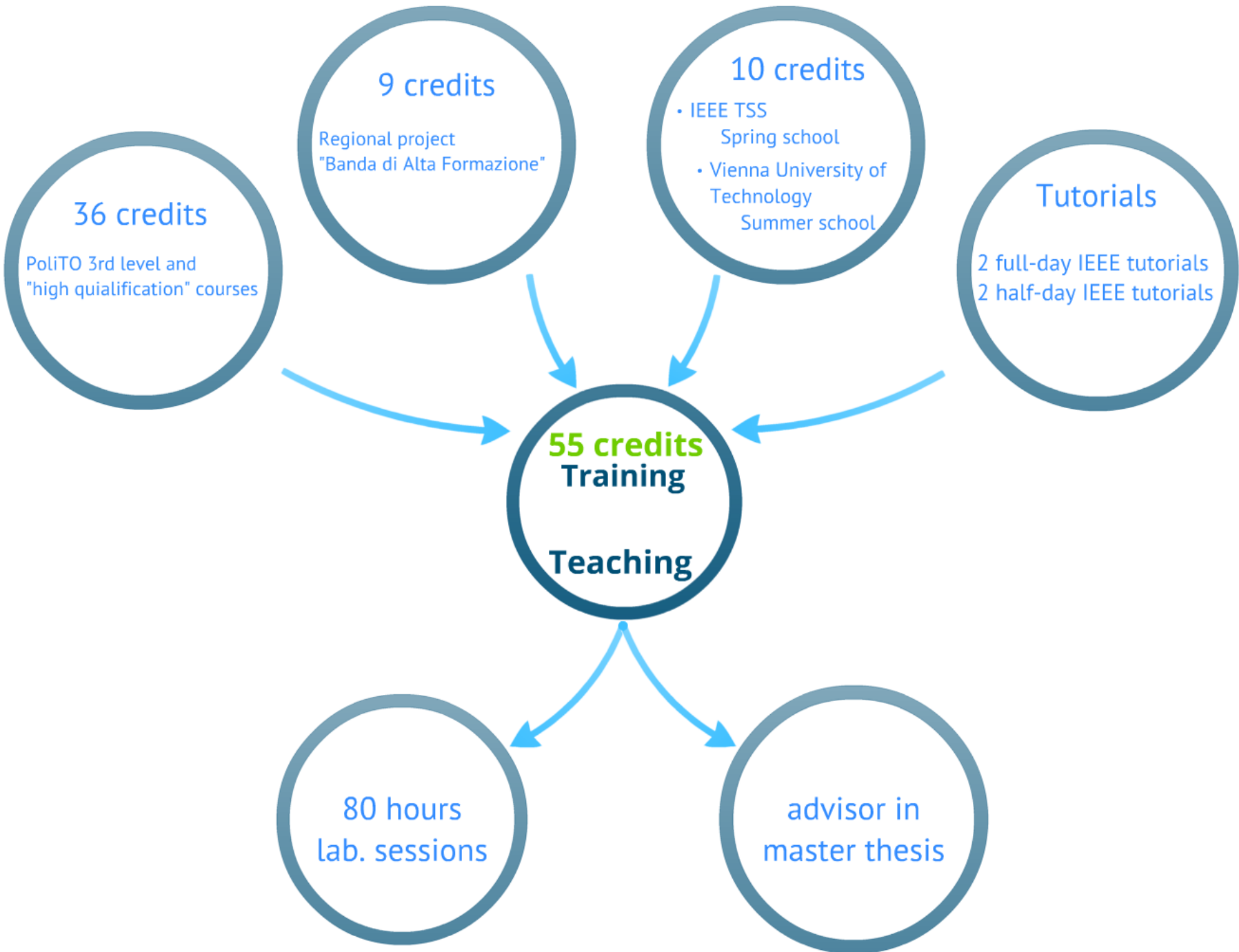
Publications & Conference participation



Collaboration with national and international industries and entities



Training and teaching activities



Conclusions

I participate actively in the **international community** and in internal **PoliTO** activities.

I developed **innovative reliability characterization techniques** for electronic circuits (microprocessors, memories, MEMS sensors, mixed signal devices); both for manufacturing and online testing.

All the knowledge acquired and generated during these years has been published in several international, peer-reviewed **journals and conference proceedings**.

Thank you!

Lyl M. Ciganda Brasca

Advisor: Paolo Bernardi
Ph.D. in Computer and Control Engineering
March 2013

