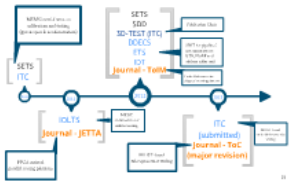
Publications & Conference participation



Collaboration with national and international industries and entities

Training and teaching activities

Conclusions

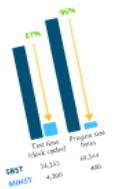
I participate actively in the international community and in internal PoliTO activities.

I developed innovative reliability characterization techniques for electronic circuits (microprocessors, memories, MEMS sensors, mixed-signal devices), both for manufacturing and online testing.

All the knowledge acquired and generated during these years has been published in several international, peer-reviewed journals and conference proceedings.

Overall miniMIPS testing results

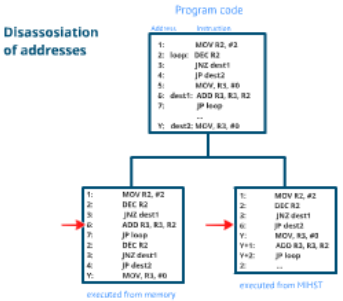
Case Study



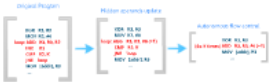
Advantages of the MIHST module

- Defect coverage
- Speed
- Confidentiality
- Robustness
- Modularity
- Ease of integration
- Limited intrusiveness
- Programmability
- Scalability
- Low cost

Disassosiation of addresses

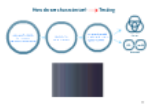


Encoding Method



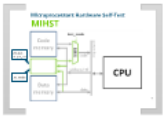
Encoding format

Example



memory is almost 50-60% of SoCs area

MIHST on-line procedure



Thank you!

New Techniques for Reliability Characterization of Electronic Circuits

Microprocessors testing issues

Thank you!

Lyl M. Ciganda Brasca

Advisor: Paolo Bernardi
Ph.D. in Computer and Control Engineering
March 2013

New Techniques for Reliability Characterization of Electronic Circuits

Reliability

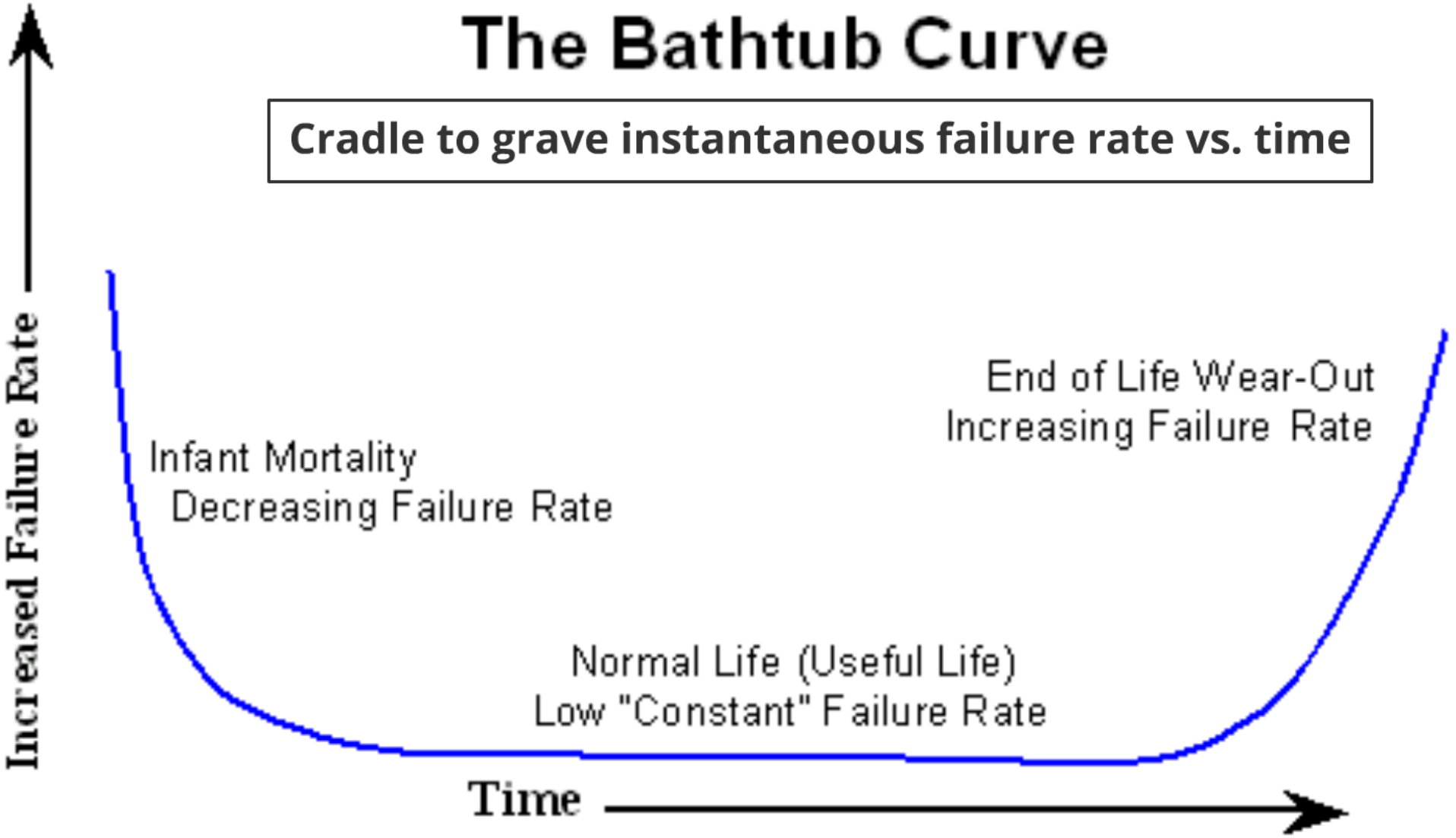
tronic Circu

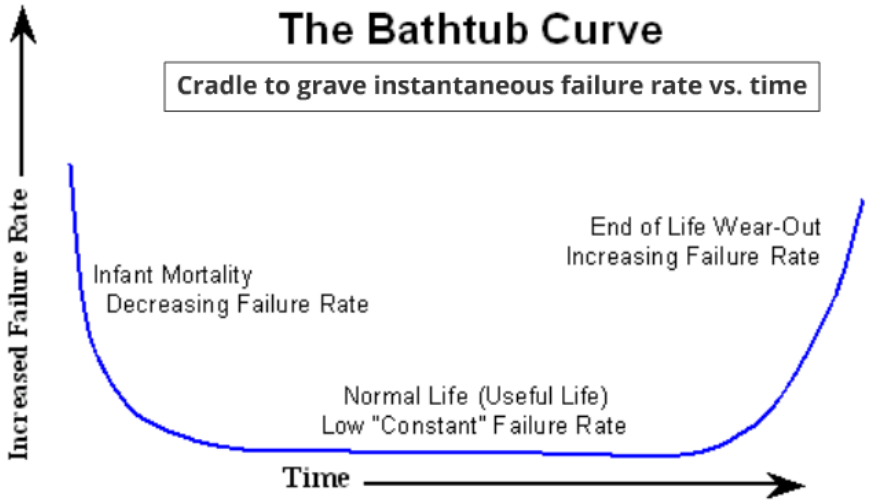
Reliability

The ability of a system or component
to perform its required functions
under stated conditions
for a specified period of time."
(IEEE Glossary)

The Bathtub Curve

Cradle to grave instantaneous failure rate vs. time





Failures causes in "Normal life"

radiation

Failures causes in "Normal life"

radiation

α rays

high-energy particles

contamination

gas

dust

environment

temperature

humidity

magnetic and

electrical fields.

maximum ratings

voltage

current density

mechanical stress

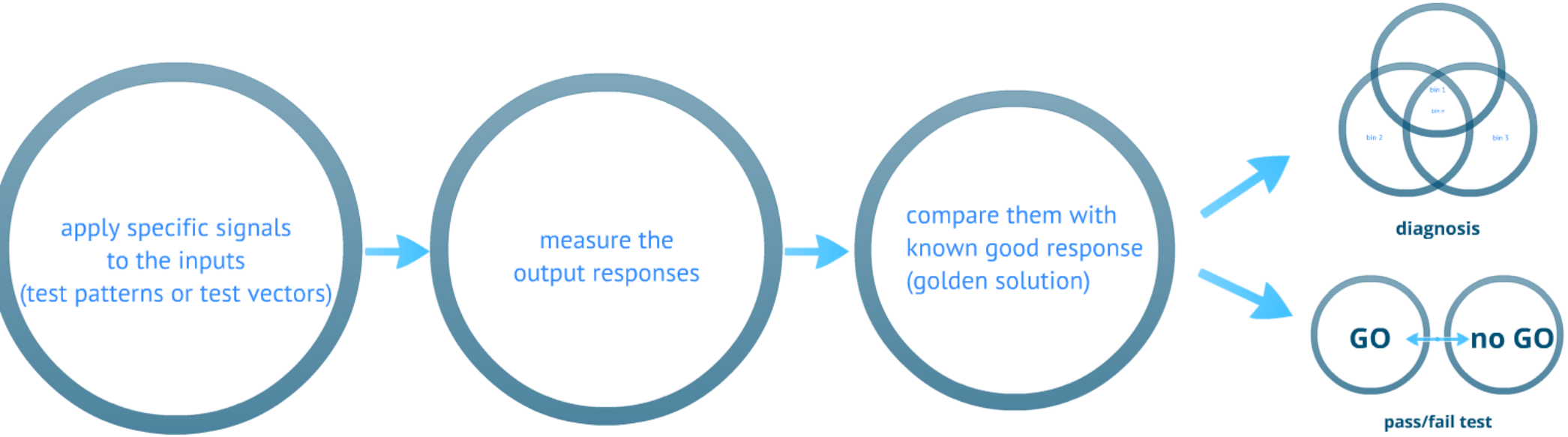
vibration

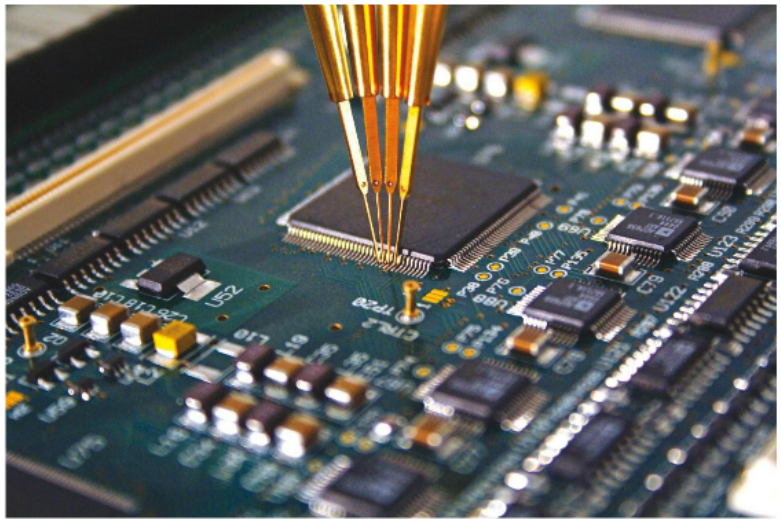
shock

pressure

New Techniq
Characterization

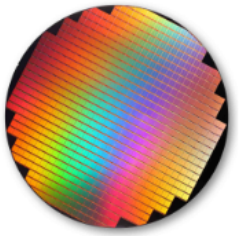
How do we characterize? → Testing





Manufacturing testing

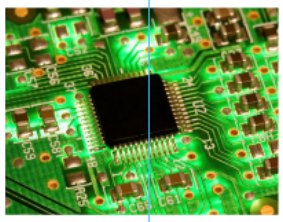
Wafer sorting



After packaging testing

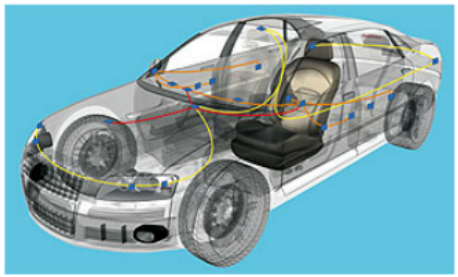
Burn in

ATE



Online testing

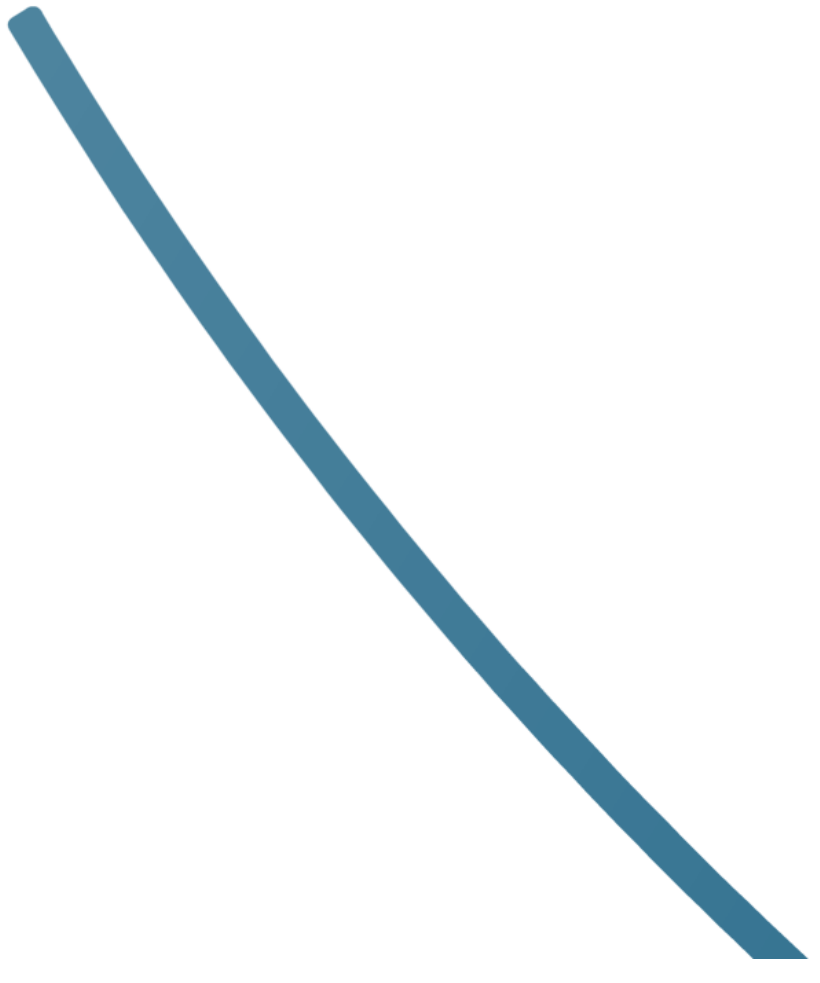
Periodic testing



On demand testing

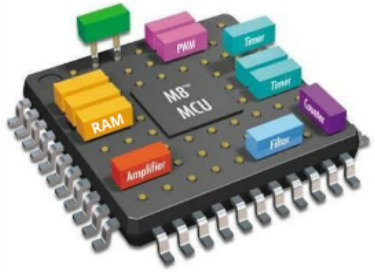
s for Reliability

Electronic Circuits



System-on-a-Chip

Microprocessors



Memories

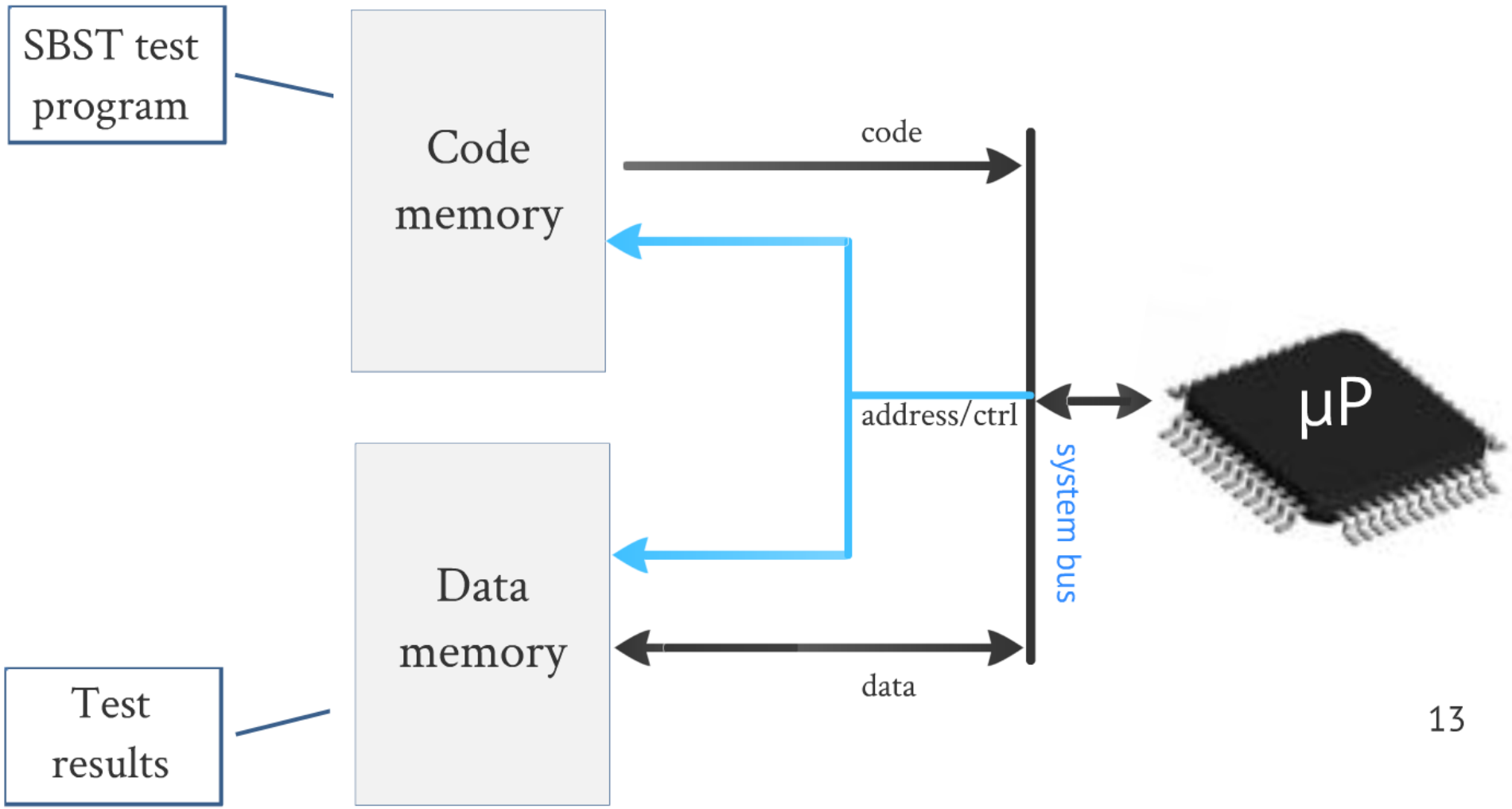
MEMS Sensors

Analog-to-digital Converters

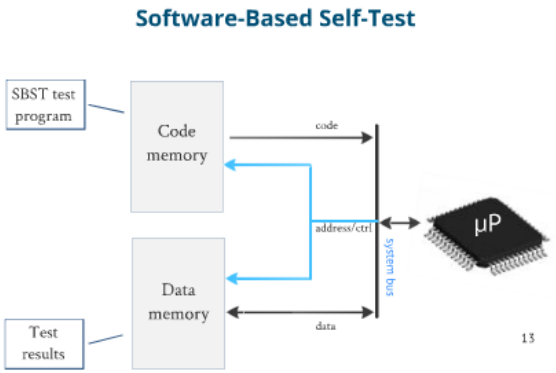
Microprocessors testing issues

- fault coverage (%)
- at (maximum) speed
- diagnostic information
- standard test access mechanisms
- area (or memory) overhead
- acceptable total test time
- Intellectual Property
- respect power consumption constraints
- respect online timing constraints
- transparent execution w.r.t.
  - system state
  - data memory content
  - dependant on system configuration
- faulty execution may lead to hazardous condition

Software-Based Self-Test



Microprocessors testing issues



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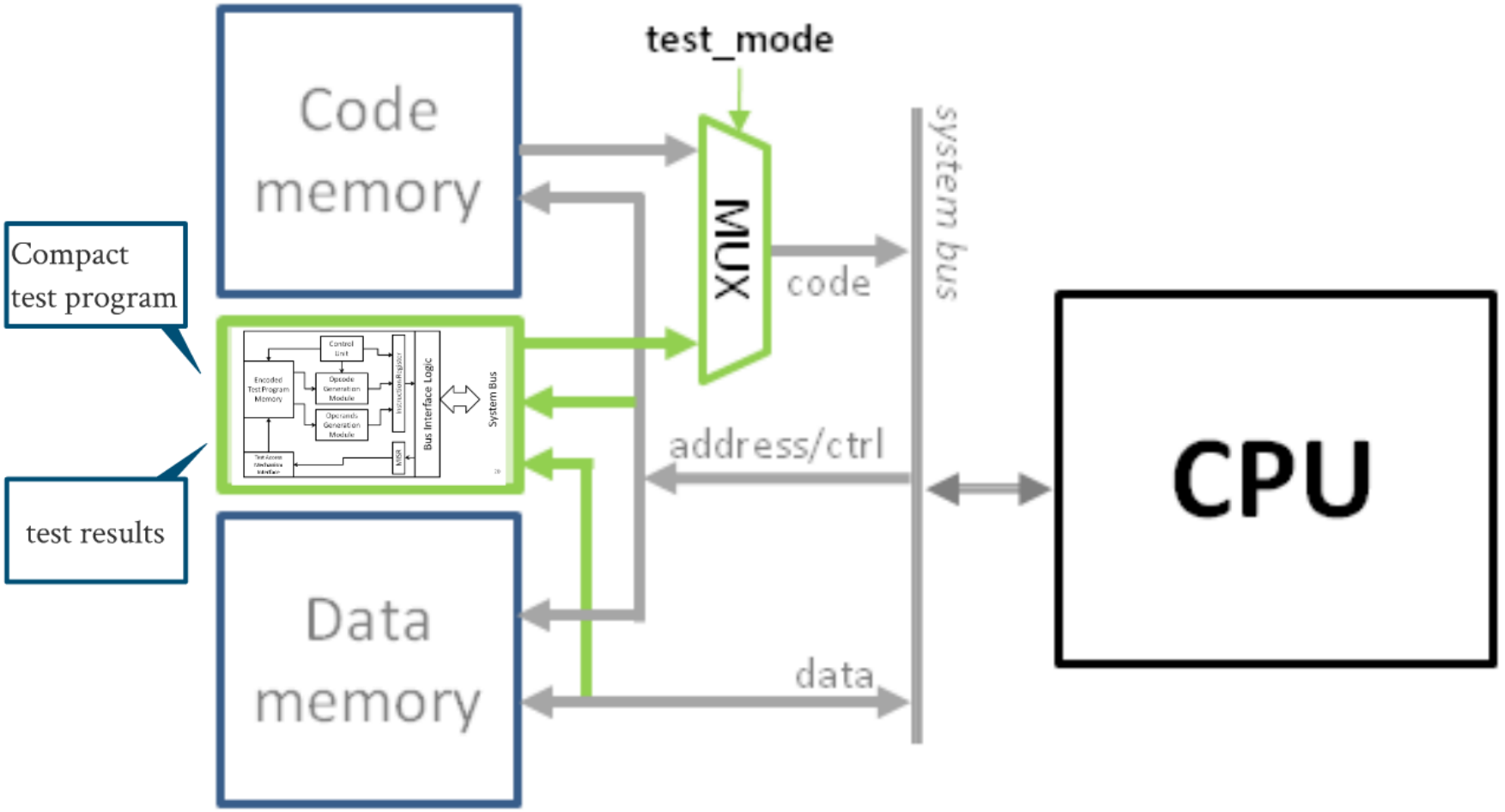
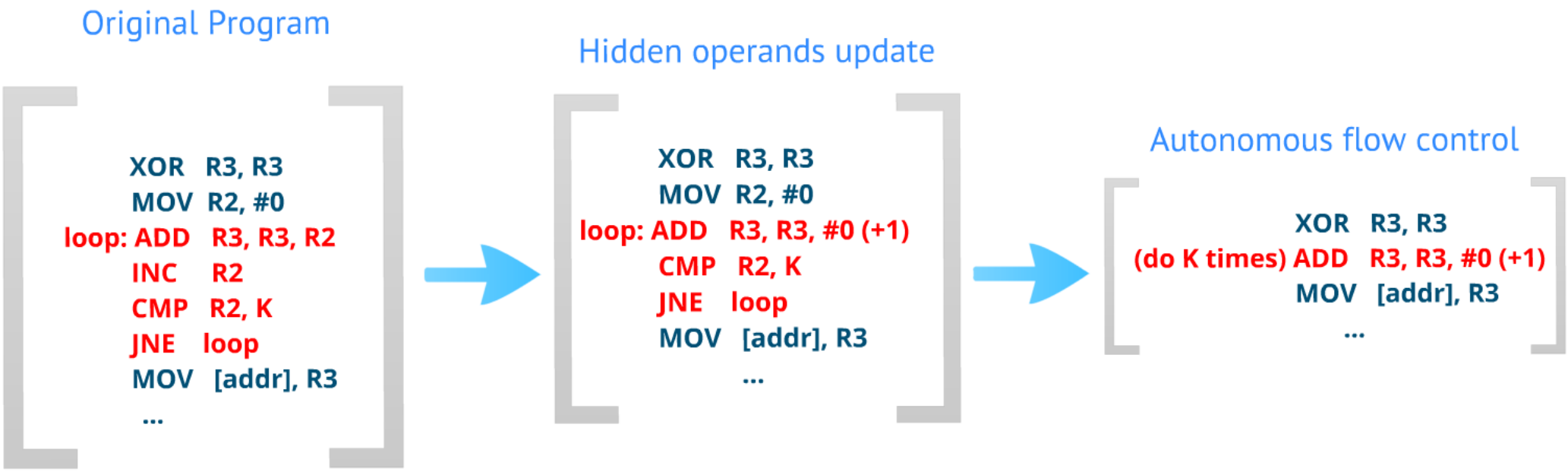
New Techniques
haracterization of E

MIcroprocessors Hardware Self-Test

MIHST



Encoding Method

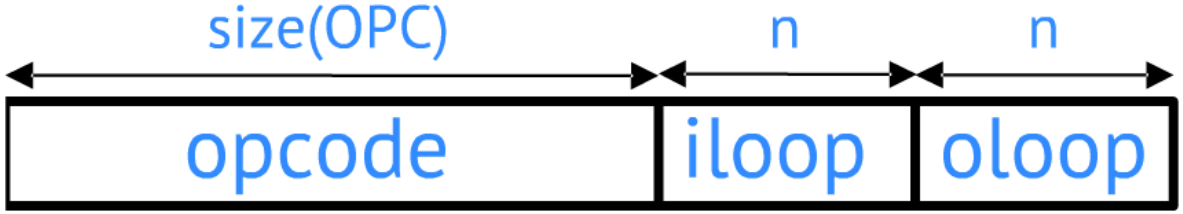


Encoding format

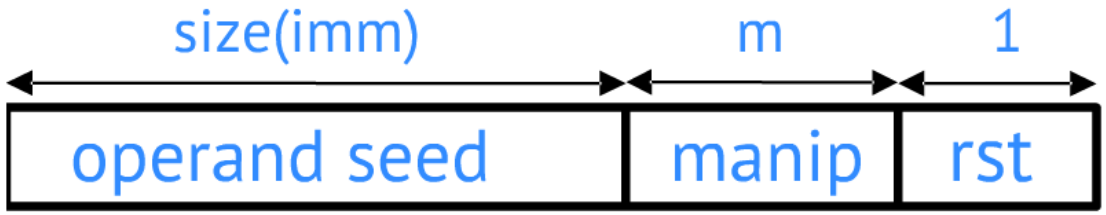
Example

Encoding format

OPCode word



OPErand word(s)



Original Program

```
XOR   R3, R3
MOV   R2, #0
loop: ADD   R3, R3, R2
INC   R2
CMP   R2, K
JNE   loop
MOV   [addr], R3
...
```

Hidden operands update

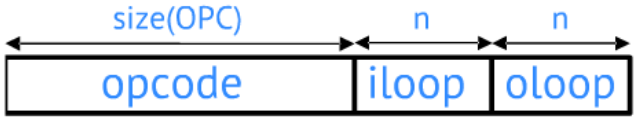
```
XOR   R3, R3
MOV   R2, #0
loop: ADD   R3, R3, #0 (+1)
CMP   R2, K
JNE   loop
MOV   [addr], R3
...
```

Autonomous flow control

```
XOR   R3, R3
(do K times) ADD   R3, R3, #0 (+1)
MOV   [addr], R3
...
```


Encoding format

OPCode word



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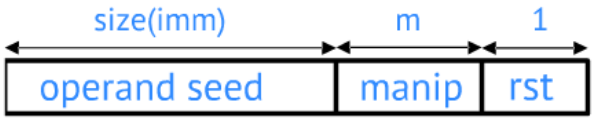
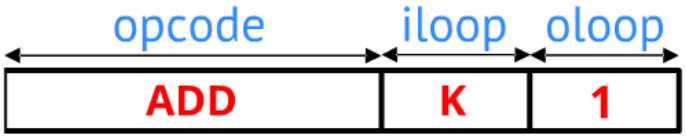


Example

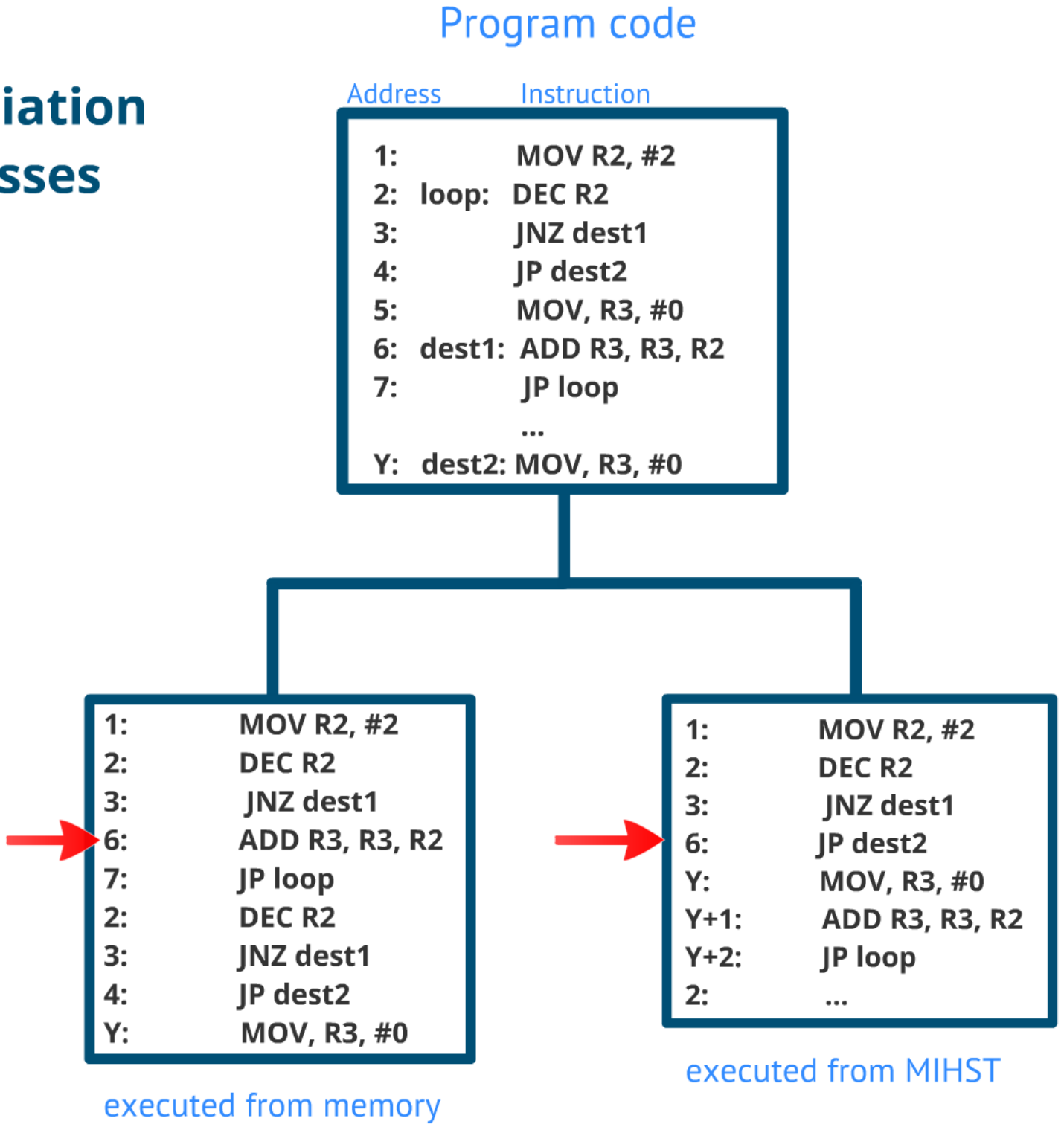
OPCode



OPErand

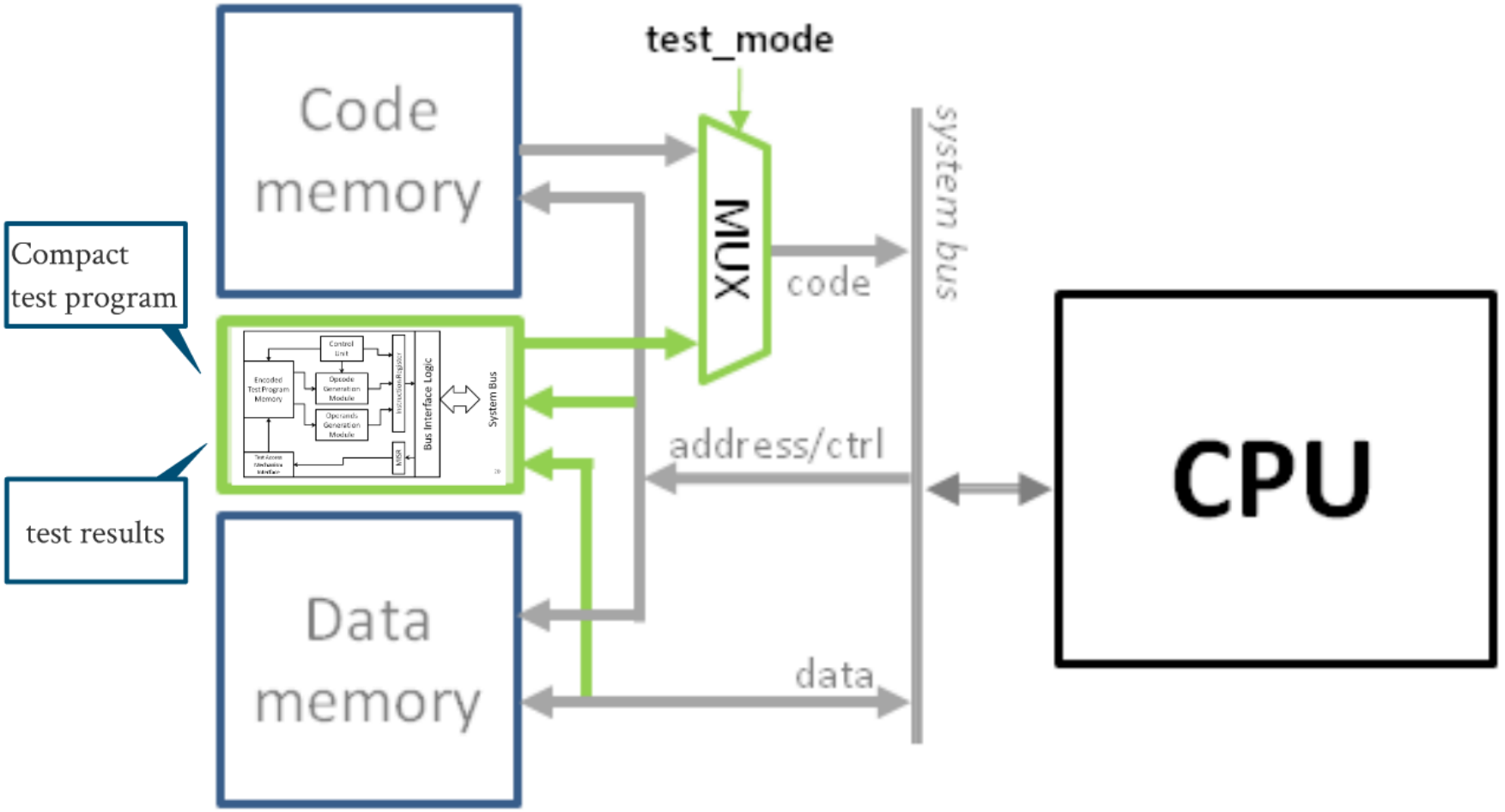
	operand seed	manip	rst
1	R3	-	
2	R3	-	
3	0	inc	1

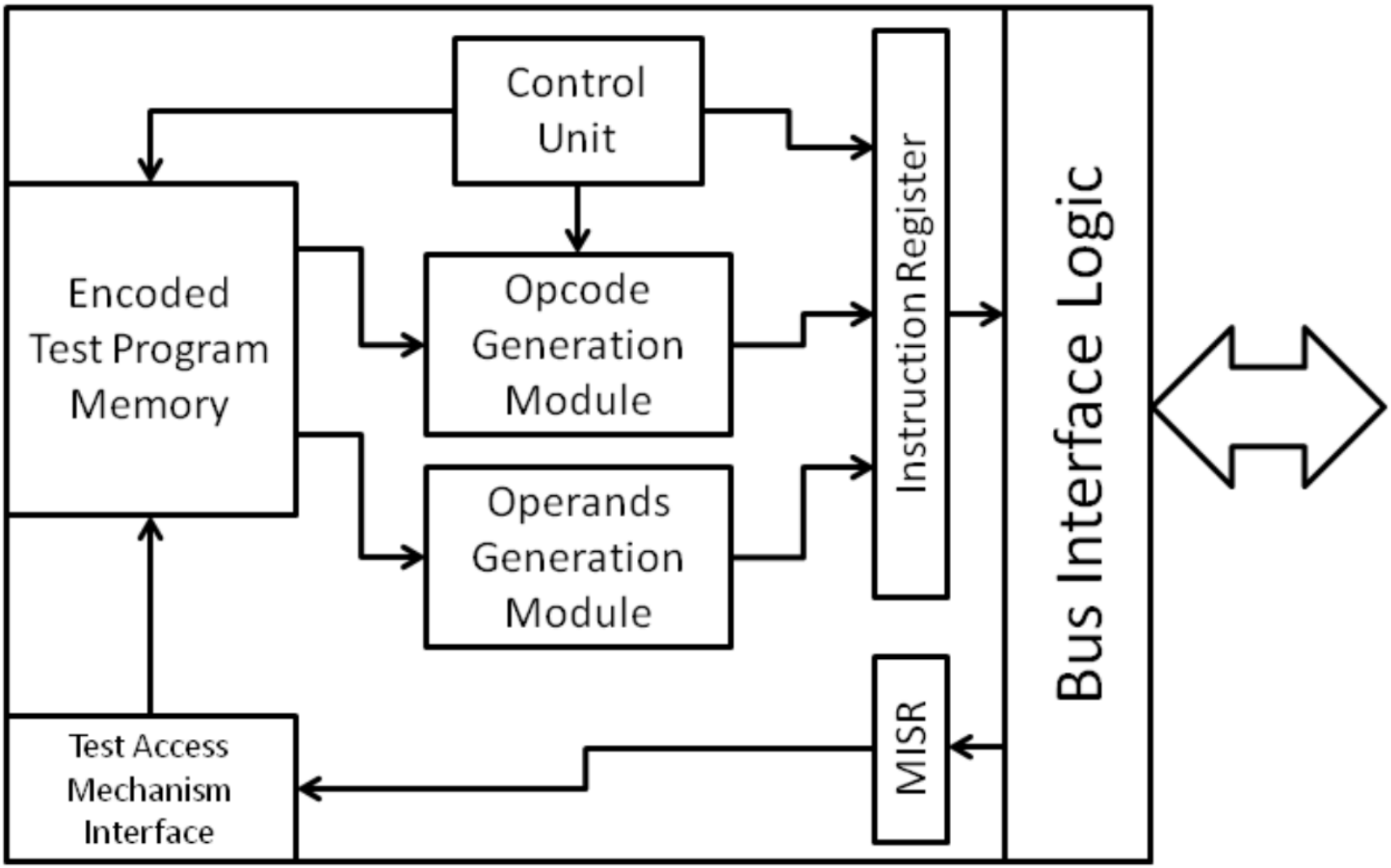
Disassosiation of addresses



MIcroprocessors Hardware Self-Test

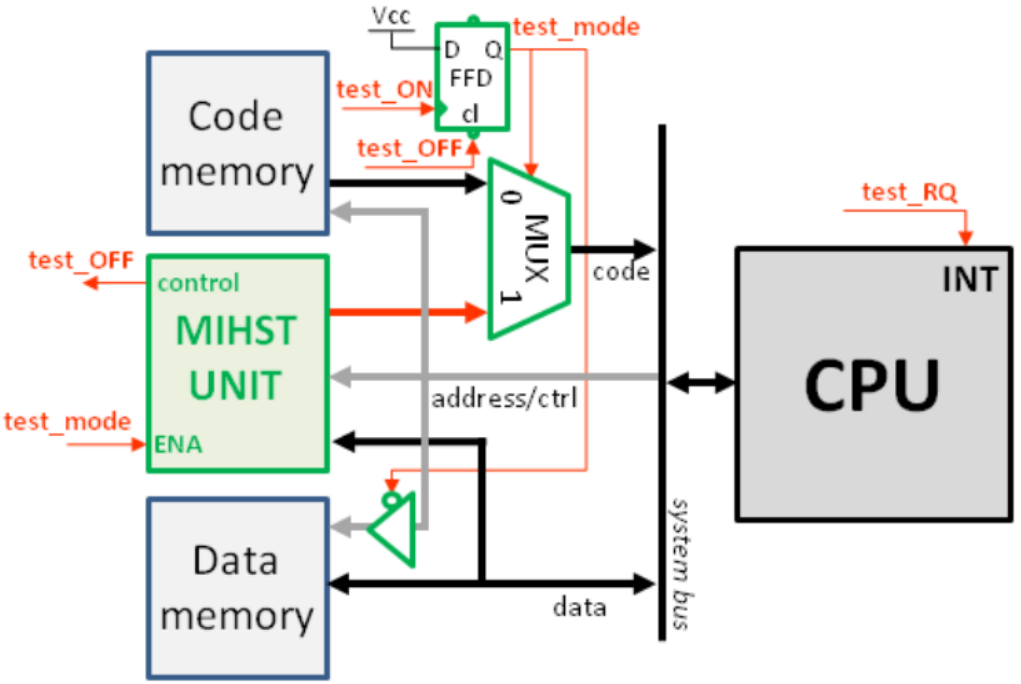
MIHST




Control Unit
Encoded Test Program Memory
Opcode Generation Module
Operands Generation Module
Instruction Register
Bus Interface Logic
System Bus
Test Access Mechanism Interface
MISR

MIHST on-line procedure

0. START The on-line test interrupt signal is activated
1. • The microprocessor unit saves the system context .
2. • The system control is given to the ISR, which:
   - stores all the GPRs the test program uses,
   - activates the test_mode signal (enables the MIHST module).
3. • Control is given to the MIHST module, which:
   - cleans the pipeline (NOPs),
   - reproduces the compacted test program,
   - aligns the pipeline (NOPs),
   - generates a "jump N" instruction for the CPU,
   - resets the test_mode signal and disables the MIHST module.
4. • Control is given back to the ISR, which:
   - restores the GPR contents,
   - executes the Return From Interrupt instruction.
5. END The microprocessor restores the system context and resumes its latter task.



Case Study

miniMIPS processor

- 5 stages
- 32-bit data bus
- 32-bit address bus
- 22,208 cells

MIHST unit

- 28 bits OPCode words
- 23 bits regiter OPErand words
- 7 bits immediate OPErand words
- 72-bit MISR module
- 3,590 cells

Overall miniMIPS testing results

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- 72-bit MISR module
- 3,590 cells

22

	Test time (clock cycles)	Progam size bytes
SBST	34,233	10,344
MIHST	4,200	400

Advantages of the MIHST module

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- Speed
- Confidentiality
- Robustness
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- Ease of integration
- Limited intrusiveness
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- Scalability
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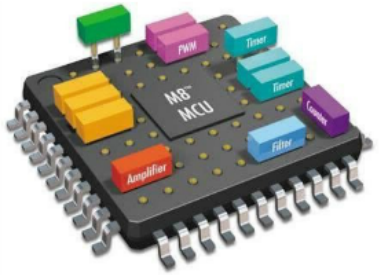

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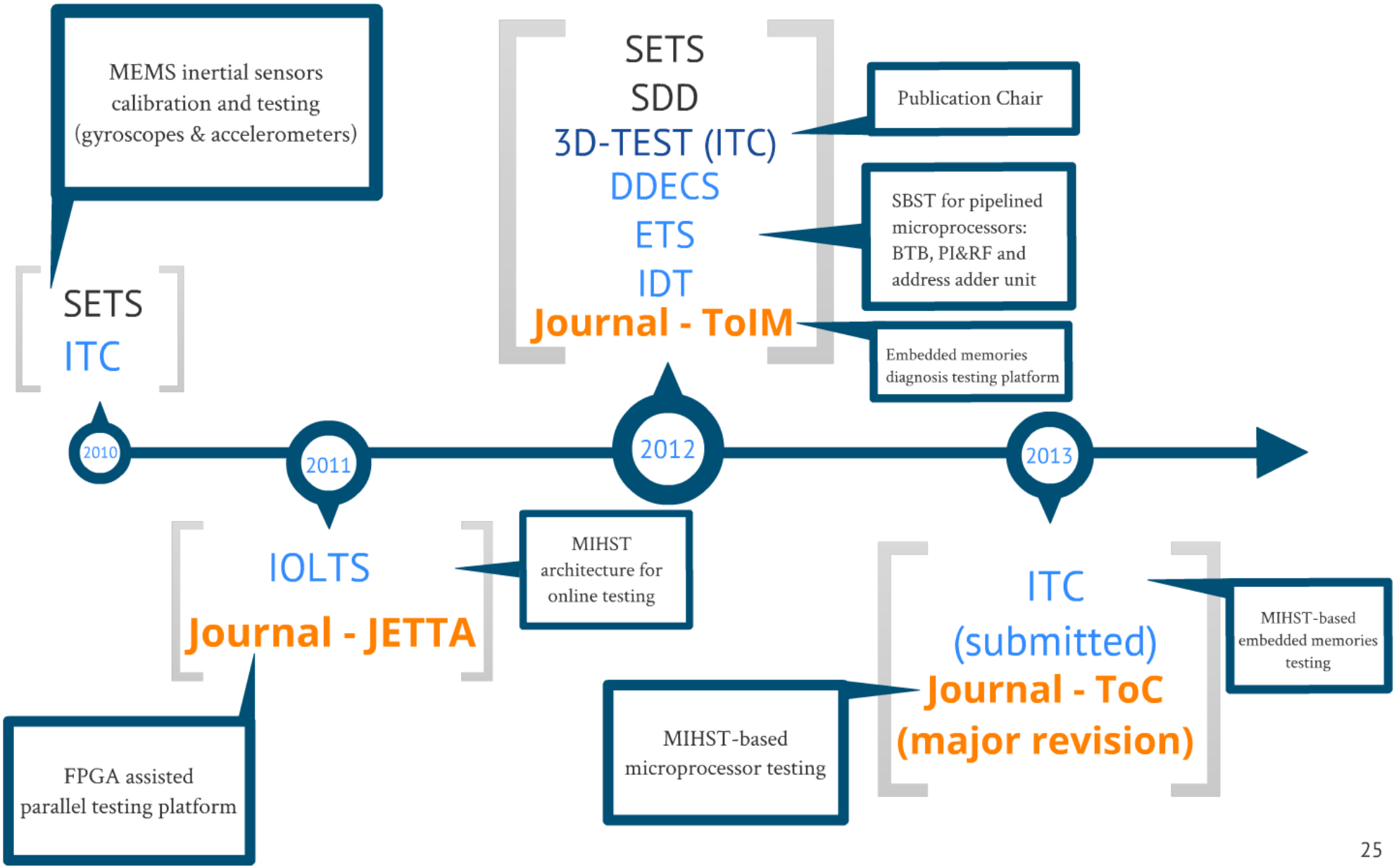

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