New Test and Fault Tolerance Techniques for Reliability Characterization of Parallel and Reconfigurable Processors

PhD Final Exam presentation

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Motivations and Goals

• Parallel and reconfigurable systems are more and more used in a wide number of applications and environments, ranging from mobile devices to safety-critical products
  • reliability needs increase continuously

• New test and fault tolerance techniques are proposed
  • addressing the most common parallel and reconfigurable computational units...
  • ...today used in mission-critical and safety-critical devices.
Outline

• Very Long Instruction Word (VLIW) Processors
  • test algorithms and diagnosis methods

• General Purpose Graphic Processing Units (GPGPUs)
  • reliability evaluation of memories and of different device configurations

• Company collaboration: General Motors Powertrain Europe
  • project overview
  • developed tasks

• Conclusions and future works.
VLIW introduction

- Static scheduling of the operations
  - compile time detection of the Instruction Level Parallelism

+ lower power consumption
+ smaller size and complexity of the processor

- higher complexity of the compiler and of the assembly code.
VLIW applications

- used in systems demanding data intensive computations and low power consumption
  - e.g., AMD GPGPU Stream Cores (Radeon HD 5000 series)
- used even for mission-critical applications (space)
  - Tilera TILE 64 processor (64 VLIW cores)
    - image analysis onboard a Mars rover for NASA space missions.
VLIW: test methods

• Testing processor module with respect to permanent faults is an issue
• Functional test approaches (SBST) are used
• A new method aimed at the automatic generation of optimized SBST programs for VLIW processors has been developed
  • high fault coverage on all the Functional Units of a generic VLIW processor...
  • ...reducing the test time and the test program size.
VLIW: test methods

• testing processor module with respect to permanent faults is an issue
• functional test approaches (SBST) are used
• a new method aimed at the automatic generation of optimized SBST programs for VLIW processors has been developed

• This work has been developed partially in the 1st year and partially in the 2nd year of PhD
• Published in a journal paper: IEEE Transactions on Very Large Scale Integration (VLSI), April 2013.
VLIW: diagnosis method

- When VLIW processors dependability is a concern, dynamic reconfiguration is used
  - permanent fault detection
  - fault location
  - repair

- A new method for the generation of Diagnostic Test Programs for VLIW processors has been developed
  - exploiting the SBST methods developed in the previous years of PhD
  - able to identify the faulty module
  - on a selected case study (e.g., p-VEX processor from Delft University of Technology) the faulty module is identified in about 87% of the cases.
VLIW: diagnosis method

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  - permanent fault detection
  - fault location
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Published in:
- conference paper (IFIP/IEEE VLSI-SoC 2013)
- Springer Book Chapter, 2013.
GPGPUs Introduction

• GPGPUs are increasingly adopted and preferred to CPUs in:
  • several computationally intensive applications (not necessarily related to computer graphics)
  • safety-critical applications, i.e., automotive (Advanced Driver Assistance Systems - ADAS), biomedical, avionics, etc...
  • High Performance Computing (HPC)

• The GPGPUs reliability is currently a hot research topic

• NVIDIA Fermi architecture: one of the most frequently adopted architectures.
GPGPU: radiation tests

- Main goal: evaluation of soft-error effects in GPGPU applications

- Three Neutron-based tests campaigns
  - ISIS facility (Didcot, UK), May and December 2013
  - LANSCE facility (Los Alamos, USA), August 2013

- Target Device:
  - NVIDIA Quadro 1000m.

ISIS test facility →
GPGPU: radiation tests

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Collaboration with Professors Paolo Rech and Luigi Carro from Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil.
GPGPU: radiation tests

1. evaluation of the radiation sensitiveness of the L1 and L2 caches
   • measurement of the Failure In Time (FIT)

2. evaluation of traditional soft-error detection techniques applied to GPGPUs code
   • time redundancy
     • Detected errors: 87.5% / Overhead 97.5%
   • thread redundancy
     • Detected errors: 75.1% / Overhead: 4.11%
GPGPU: radiation tests

1. evaluation of the radiation sensitiveness of the L1 and L2 caches
   • measurement of the Failure In Time (FIT)

2. evaluation of traditional soft-error detection techniques applied to GPGPUs code

Published Papers:


• On the evaluation of soft–errors detection techniques for GPGPUs, *IEEE International Design and Test Symposium (IDT)*, December 2013.
GPGPU: radiation tests

3. FFT algorithm
   • based on the Cooley–Tukey algorithm
   • Three different GPGPU configurations:
     • FFT_64: 2 Thread Blocks with 64 Threads in each block
     • FFT_32: 2 Thread Blocks with 32 Threads in each block
     • FFT_64_NOL1: 2 Thread Blocks with 64 Threads in each block, cache L1 disabled.

• The most reliable configuration has been obtained by disabling the L1 caches
  • limited performance degradation, in the case of FFT algorithm.
GPGPU: radiation tests

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Published Paper:

degradation, in the case of FFT algorithm.
GM activity: project overview

• **Project GOAL**: performance and reliability evaluation of a new Timer Module (i.e., the Generic Timer Module) used in automotive domain

• Utilization Context:

![Diagram of CrankShaft, CamShaft, and Cylinders Injection Pulses connected to a Timer Module (GTM)]
GM activity: 3 performed tasks

1. Timer Module programming
   • 7 functions (required by GM) managing the engine fuel injection
   • SPC574k Freescale / ST evaluation board

2. Development of an FPGA-based validation platform
   - Xilinx Virtex 5
   - Microblaze processor

3. Experiment campaigns:
   • detailed analysis with different engine behavior.
Conclusions and Future Works

- **3 activities**
  - 2 research activities (VLIWs and GPGPUs reliability)
  - 1 company collaboration (GM Powertrain)

- **16 published papers**
  - 3 journal papers
  - 1 Springer book chapter
  - 12 international peer-reviewed conference papers

- **Future Works:**
  - VLIW: development of a partial reconfiguration environment
  - GPGPU: same techniques to different GPGPU models (e.g., AMD)
  - GM activity: possible extension of the current contract, to further investigate the GTM capabilities.
Thank you

• Any questions?