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New techniques to detect and mitigate aging effects in advanced semiconductor technologies

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1. Introduction

Advanced semiconductor technologies present more frequent physical defects and a shorter lifespan. Some of these defects cannot be tested by means of traditional fault models, as they are better modeled by delay fault models both in the form of transition and path delay faults.

2. Goal

Provide Software-Based Self-Test solutions (SBST) for delay fault models specifically to ensure the safety and reliability of the device throughout its operative lifetime, also dealing with aging.

3. Path Delay Fault solutions

No commercial fault simulation tool currently supports functional fault simulation of Self-Test Libraries for path delay faults in sequential circuits. Hence, I first developed a test flow for PDFs with a specific focus on CPUs. Thanks to this, I evaluated path delay fault coverages with state-of-the-art STLs developed for other fault models, reaching a 52% coverage in the best-case scenario [1].

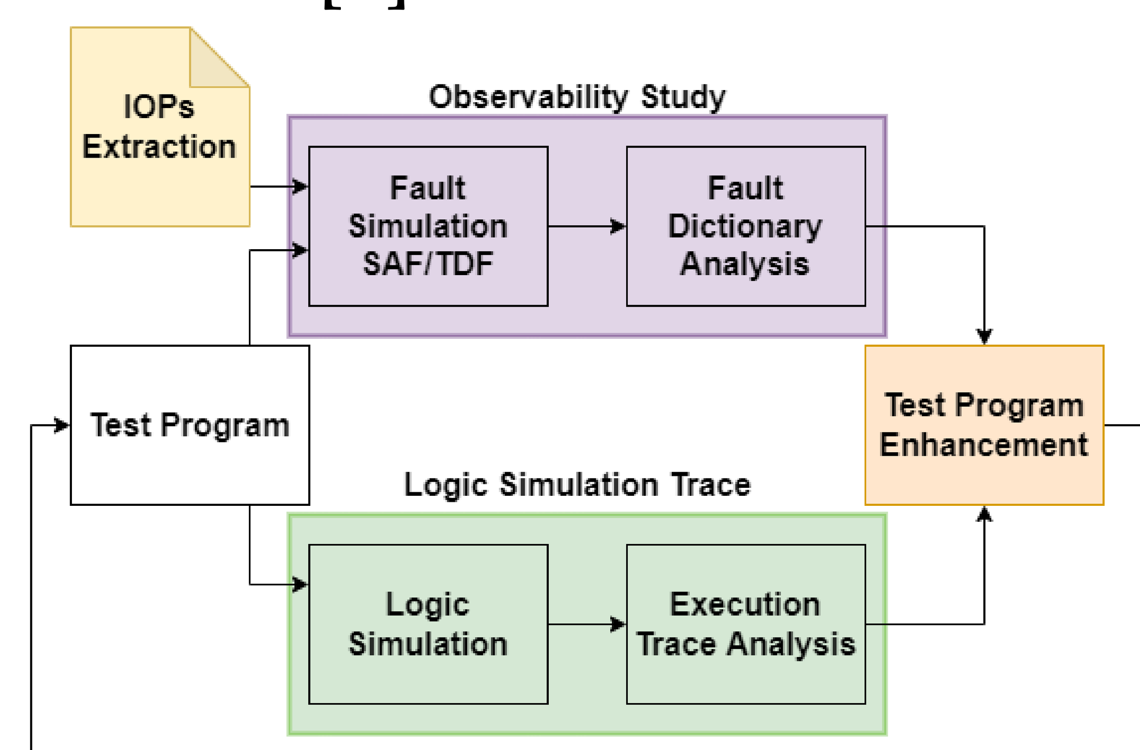
Following, I developed a systematic approach on writing STLs for PDFs. This methodology led to the detection of all testable faults affecting critical paths and 87.31% of faults affecting shorter paths.

Finally, aging is considered by increasing propagation delays of cells in the circuit based on time and adopted workload. This allows to estimate how well STLs perform in time, ensuring the correct functioning on-the-field over several years.

4. Transition Delay Fault solutions

Solutions for TDFs focus on improving fault coverages achieved by STLs by tackling not-observed transition delay faults. They consist of software and hybrid hardware-software solutions.

The software-based approach consists of an automatic flow that, given the original test program, finds a set of faults to target and hints at where the test program should be modified, together with suggestions on how to improve it. This allows to recover a significant percentage of faults with a relatively small increase in code size and execution time [2].



The hybrid solution is based on a heuristic set covering approach to select the subset of flip-flops reached by faulty values to observe through post-silicon debug hardware to reach the target fault coverage. Experimental data shows that all not-observed transition delay faults are detected through this methodology [3].

5. References

1. S. Sartoni et al. "New Perspectives on Core In-Field Path Delay Test", 2020 IEEE International Test Conference
2. S. Sartoni et al. "Effective techniques for automatically improving the transition delay fault coverage of Self-Test Libraries", 2022 IEEE European Test Symposium
3. S. Sartoni et al. "Exploiting post-silicon debug hardware to improve the fault coverage of Software Test Libraries", 2022 IEEE VLSI Test Symposium