

Vulnerability-Tolerant Architectures for Resource-Constrained Devices

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1. Context

- Control-Flow Hijacking Attacks
- Embedded Systems
- Hardware-based Security

2. Issues

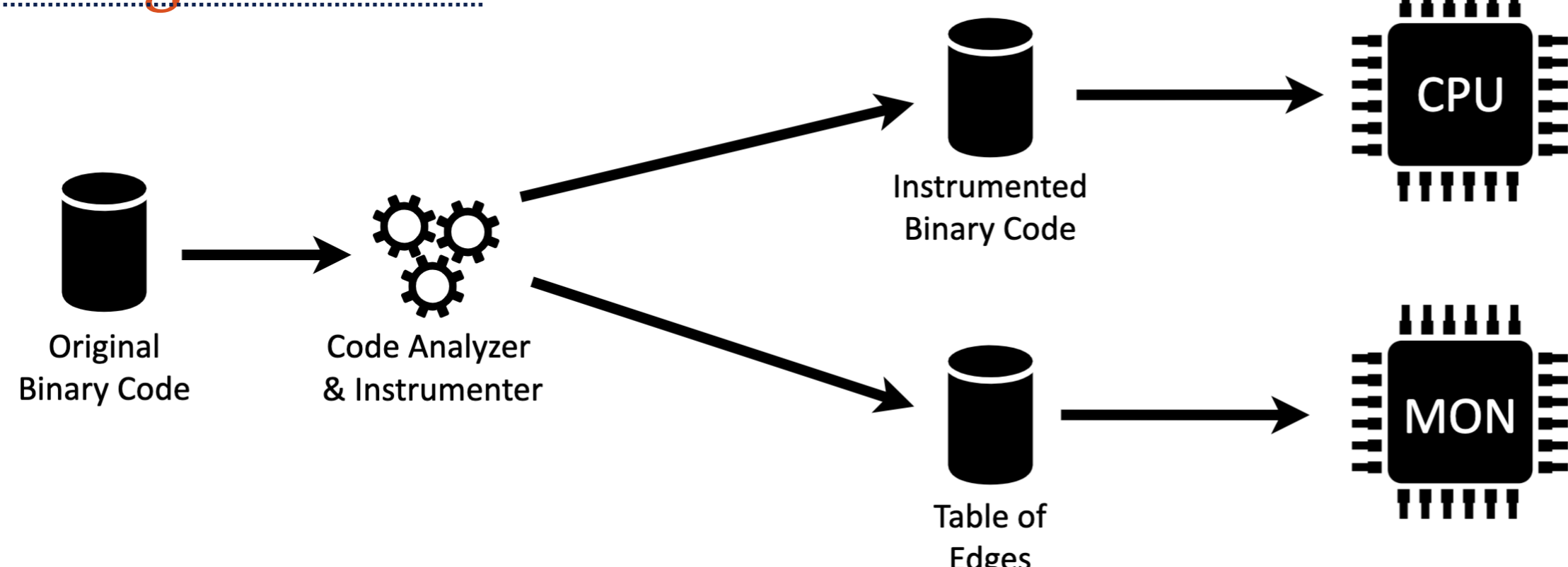
- C/C++ languages:** widely used in ES, good degree of low-level control but possible **memory vulnerabilities** for lack of native controls on pointer manipulation;
- Attackers exploit them to **corrupt code pointers** and reach random instructions at will, forcing the system to behave abnormally.

4. Our Approach

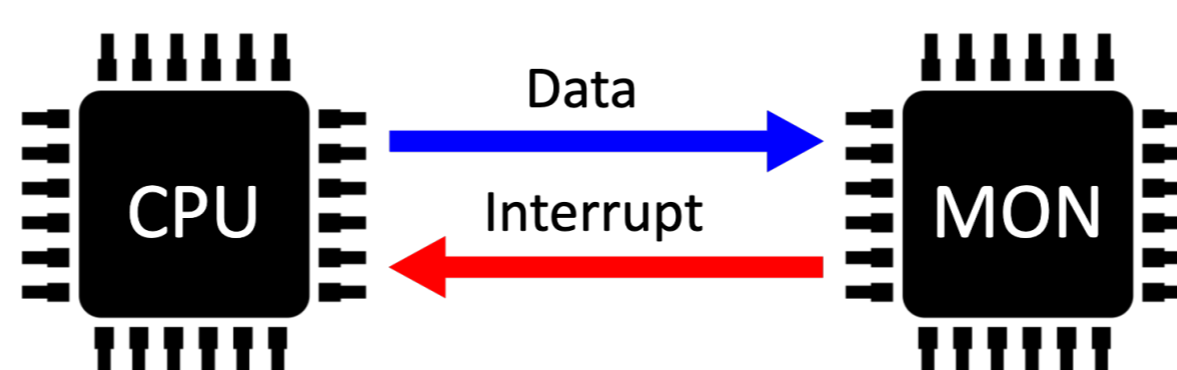
What is protected

- Indirect forward edges
- Backward edges
- Interrupt Service Routines

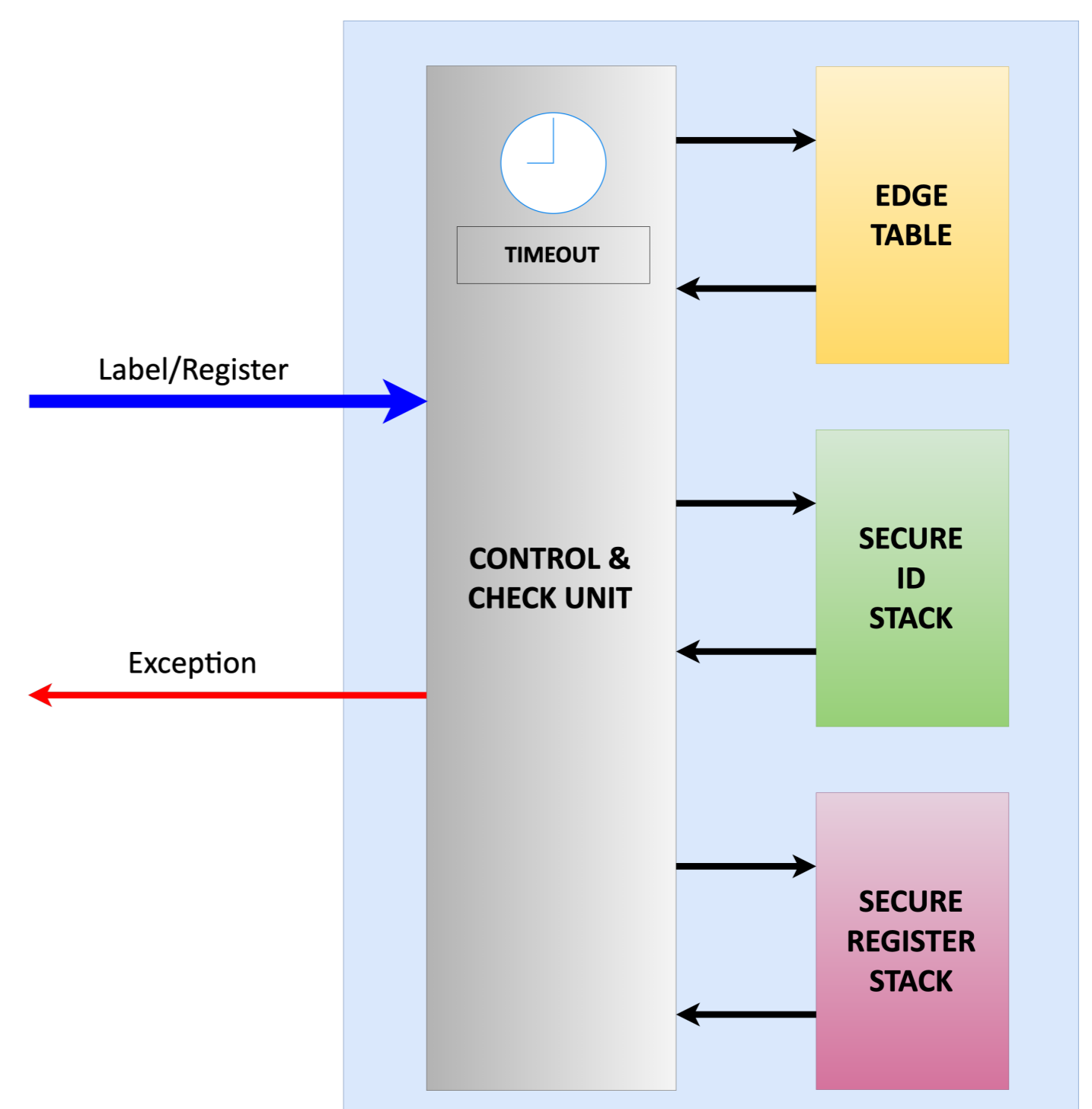
Setting the scene



How the protection works



Monitor structure



5. Experimental Results

- Solution experimented for ARM Cortex-M and 32-bit custom RISC-V processor [6]
- External parallel FPGA for ARM, internal monitor for RISC-V
- ARM: **+17.88%** on code size, **+1.10%** on execution time
- RISC-V: **+0.63%** on code size, **+0.01%** on execution time

6. References

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