life.augmented IMM Politecnico di Torino
Dipartimento di Automatica e Informatica

PhD in Computer and Control Engineering

Supervisors
Matteo Sonza Reorda
Michelangelo Grosso

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New techniques for quality and reliability enhancement in electronic systems

PhD Candidate: *NUNZIO MIRABELLA*

1. Introduction

The adoption of Cell-Aware Testing (CAT) is increasing in semiconductor companies. Past studies have extensively shown the capability of CAT to identify physical defects of those microchips that would otherwise remain undetected using traditional fault models only. Resorting to the CAT approach we can increase the overall quality of the manufacturing process by reducing the number of test escapes.

2. Goals

The goal of the research activity in collaboration with STMicroelectronics and Centro Nazionale di Ricerca (CNR) aims at the development of solutions to improve quality and reliability of electronic devices. The use of CAT produces a higher number of patterns compared with other fault models. This causes an increase in testing time on the automatic test equipment (ATE). To reduce this negative side effect, it is important to reduce the number of generated patterns and obtain the best trade-off between coverage of all faults, including traditional fault models and application time. In this work a comparison between different cell-aware testing automatic test patterns generation (CAT-ATPG) flows (Fig.1) is carried out, to allow testing engineers to assess their advantages and disadvantages.

3. Method

The flows were divided into two sets of four flows each, considering stuck-at faults (SAFs) and static-CA faults for the first set (ATPG-FLW1 to ATPG-FLW4) and TDFs and dynamic-CA faults for the second set (ATPG-FLW5 to ATPG-FLW8).

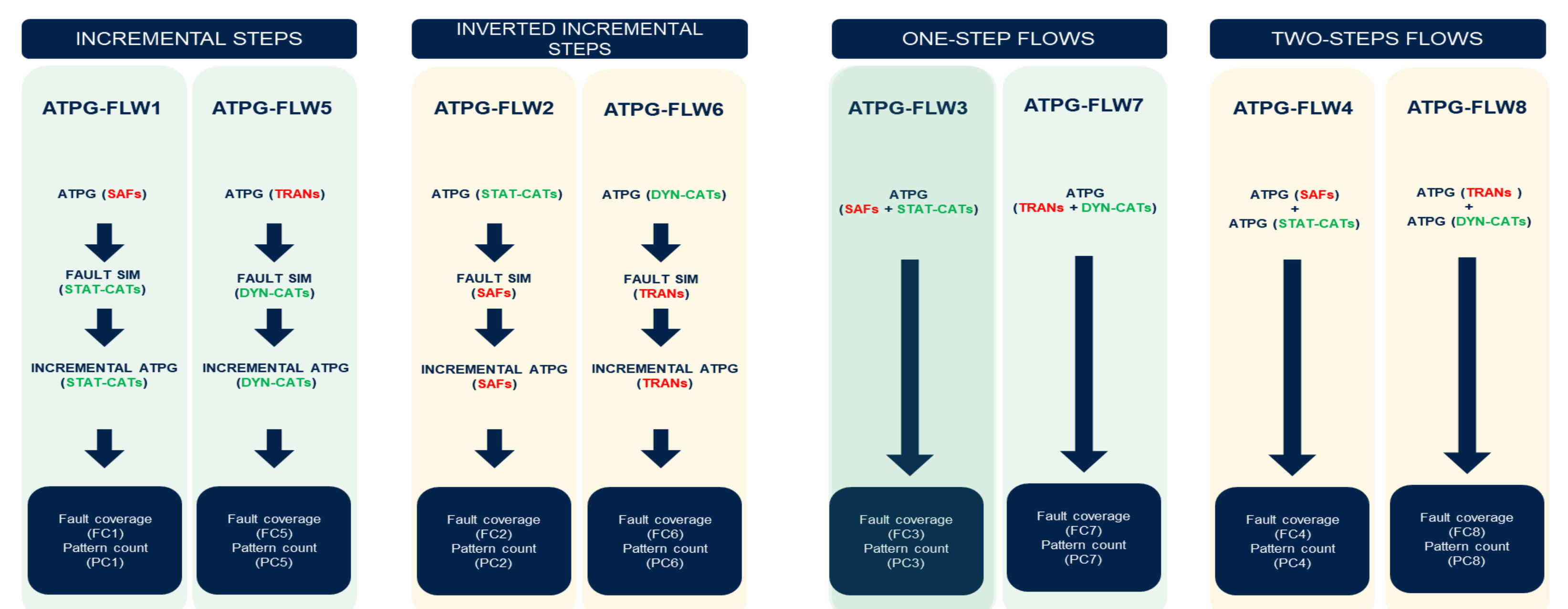

Fig. 1 – CAT-ATPG flows

4. Results

Experiments were done using the tools CMGen and TestMAX™ ATPG by Synopsys [1].

ATPG-FLW1 (Fig.2) and ATPG-FLW5 (Fig.3) produce on average up to 50% less patterns than the other flows, resulting in a reduced test application time; they would be the best choice for CAT implementation in test development flows.

ATPG-FLW4 and ATPG-FLW8 performed the worst results, due to the higher number of patterns and a lower coverage value regarding the ATPG TDF/dynamic-CAT.

Future works will involve the adoption of such flows within more complex designs and the evaluation of the test escapes on real STMicroelectronics devices [2].

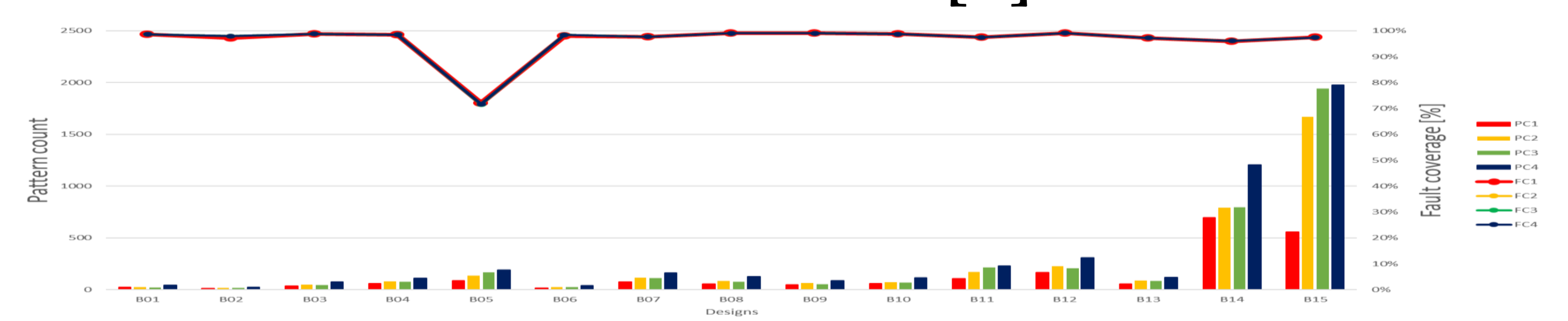

Fig. 2 – SAFs & Static-CAT ATPG flows results

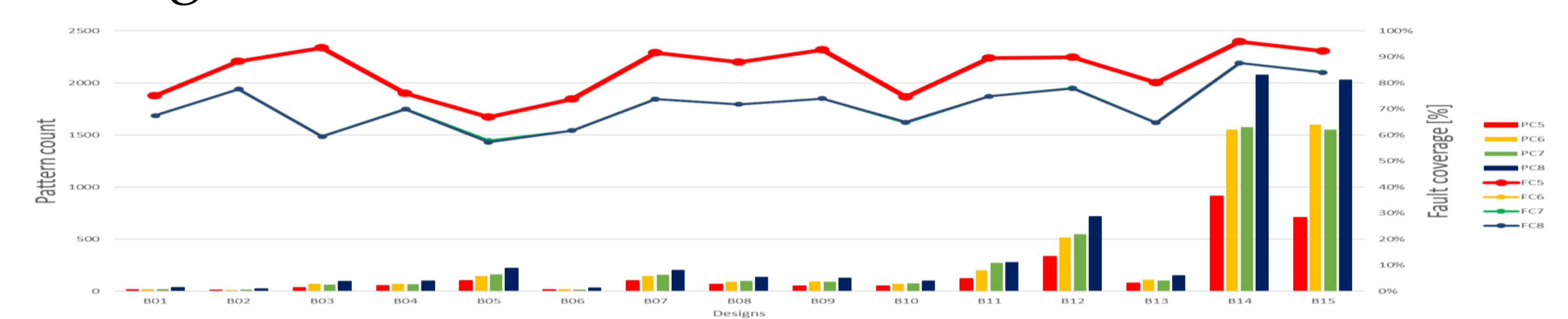

Fig. 3 – TRANs & Dynamic-CAT ATPG flows results

5. References

1. P. Bernardi et al., "Recent Trends and Perspectives on Defect-Oriented Testing," 2022 IEEE 28th International Symposium on On-Line Testing and Robust System Design (IOLTS), 2022.
2. MIRABELLA, Nunzio, et al. "An Experimental Evaluation of Resistive Defects and Different Testing Solutions in Low-Power Back-Biased SRAM Cells". Electronics, 2022.