Politecnico di Torino
Dipartimento di Automatica e Informatica

PhD in Computer and Control Engineering
XXXVI cycle

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Formal Techniques for Test and Reliability

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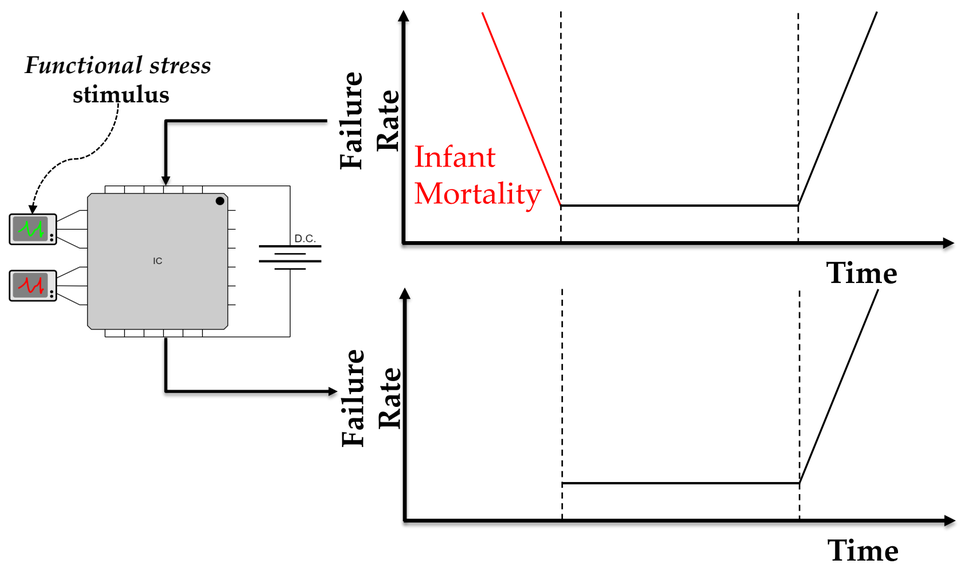
1. Introduction

Complex digital circuits have become widespread and are widely adopted in various industry and business sectors. For the safety-critical sector, one key testing procedure used in order to counter the "infant mortality" phenomenon is Burn-In test.

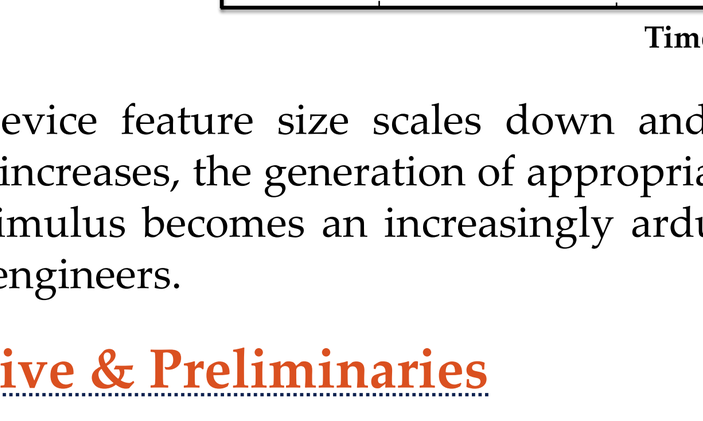


As the device feature size scales down and the test complexity increases, the generation of appropriate stress-inducing stimulus becomes an increasingly arduous task for the test engineers.

2. Objective & Preliminaries

The goal of my work, is to automate the process of the generation of stress-inducing stimuli for processor circuits. In other words, we want to maximize the number of logical switches from Low-To-High (LH) and High-To-Low(LH) over a predefined time-period for a processor module.

Given (i) a processor module **T** composed of **m** nets and (ii) the processor's Instruction Set Architecture, we aim to generate a repeatable sequence (**S**) composed of 2 instructions that maximizes the switching activity (SWA) i.e., the number of HL and LH transitions of the **m** nets when applied to **T** in a constant and repeatable manner. The process can be interpreted as a finite state machine:

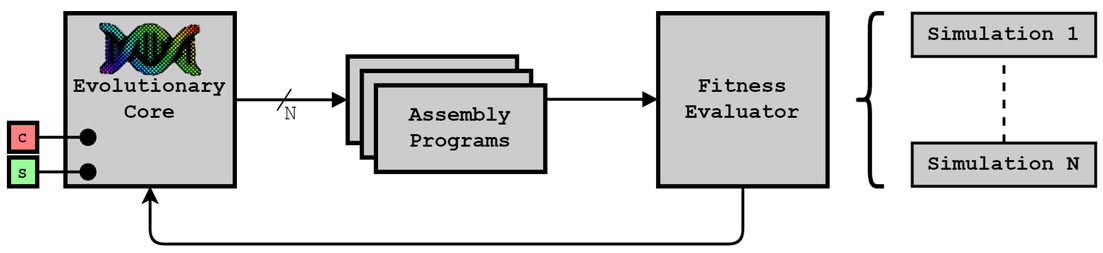


The effectiveness of a sequence S composed of **n** instructions is measured by the average induced stress metric:

$$\overline{stress}_{\%} = \frac{\sum_{i=1}^{m}[LH(i)+HL(i)]}{n \times m} \times 100$$

3. Proposed Methods

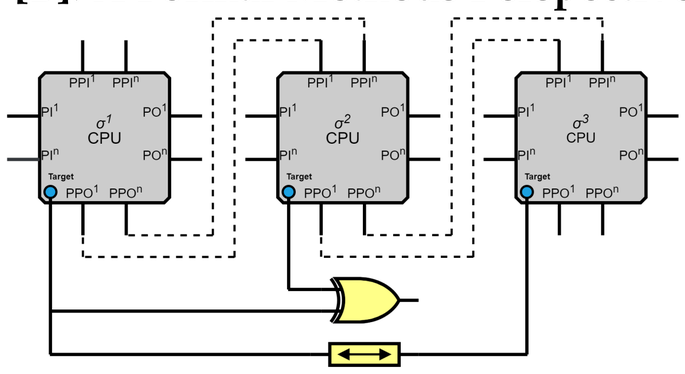
[A]: An Evolutionary Perspective



In [1] we propose a method based on the evolutionary paradigm able to effectively tackle to problem of the repeatable SWA maximization within microprocessor modules.

- ⊕ Requires a basic knowledge of the processor's ISA.
- ⊖ Does not guarantee an optimal solution.

[B]: A Formal Methods Perspective



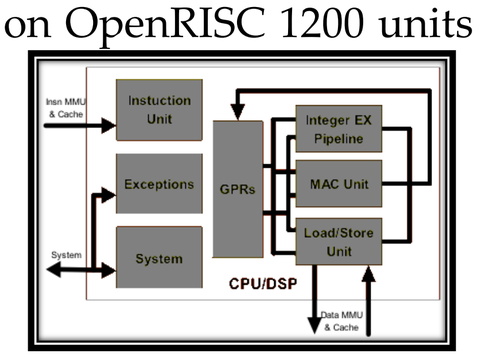
In [2] we propose a method based on formal methods (weighted max-satisfiability) able to optimally solve the problem of SWA maximization.

- ⊕ Guarantees the best/optimal solution.
- ⊖ Requires an in-depth knowledge of the architecture.

4. Results

Experimental results gathered on OpenRISC 1200 units while targeting as stress targets:

- The 32-bit adder
- The 32-bit multiplier
- The instruction decode unit
- The load and store unit.



Generation Approach	Average Induced Stress			
	Adder	Multiplier	Decoding Unit	Load Store Unit
MaxSAT	81.92%	62.15%	90.56%	65.00%
Evo	61.34%	53.77%	62.57%	58.00%
Test Program	24.00%	6.34%	44.43%	57.00%

5. References

1. N. I. Deligiannis et al. "Maximizing the Switching Activity of Different Modules Within a Processor Core via Evolutionary Techniques" in Euromicro Digital System Design (2021).
2. N. I. Deligiannis et al. "Effective SAT-based Solutions for Generating Functional Sequences Maximizing the Sustained Switching Activity in a Pipelined Processor" in IEEE Asian Test Symposium (2021).