



Reliability Evaluation and Hardening of Nano-scale SoC

PhD Candidate:

Weitao Yang (weitao.yang@polito.it)

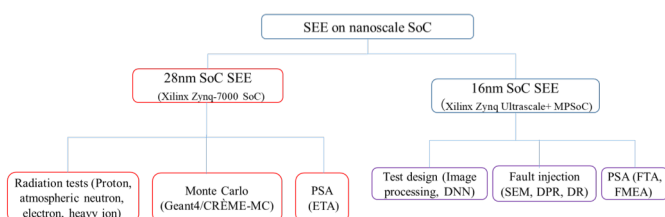
1. Introduction / Context

Nano-scale system on chip (SoC) has many advantages, making them increasingly popular in a variety of safety-critical applications, such as aerospace. However, SoC in these applications faces a hazard: the reliability problem, such as single event effect(SEE) under strong radiation environments. And smaller technology products suffer more seriously. SEEs are evaluated in different ways on two MPSoCs in my project. And some ideas and solutions are proposed



- Assess SEE vulnerability of nano-scale SoCs in different radiative environments using irradiation tests.
- Propose and verify a high efficiency SEE hardening solution.
- Combining fault injection and probabilistic safety analysis (PSA) to comprehensively evaluate SEE on SoC.
- Explore positive contribution from SEE on designs implemented on SoCs.

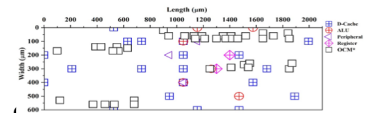
3. Schematic of the research



ETA: event tree analysis, SEM: soft error mitigation, DPR:dynamic partial reconfiguration, FTA: fault tree analysis, FMEA: failure mode and effect analysis, DNN: deep neural network
(Open source DNN, ZyNet for handwritten digital data recognition)

4. Contents

- Soft error rates of multi processor and data accessing modes are evaluated using heavy ion irradiation.
- Microbeam heavy ion and event tree analysis to study SEE propagation in a complex SoC.
- Fault injection and fault tree analysis and failure mode and effect analysis to investigate soft error influence.
- Fault injection to explore SEE positive effect on DNN designs.



Network	MN at original	MN at OEIA	Enhancement
30(G)	445	419	5.84%
31(1)	432	399	7.64%
31(2)	413	377	8.72%
31(3)	396	380	4.04%
31(4)	384	363	5.47%

MN: misidentification number, OEIA: optimal enhancement of the identification accuracy

5. Results

- ✓ The processor mode has no influence on single event upset, while the soft error ratio is 5.13:1 between the static and dynamic modes.
- ✓ The probability of SEE propagation from one to another one, two and three blocks at 10^{-8} , 10^{-12} and 10^{-17} levels, respectively[1].
- ✓ SEE in some locations in the configuration memory can improve DNN identification accuracy. And there are one or more bit can make this improvement maximum.
- ✓ An solution is proposed to improve DNN performance based on fault injection and optimal fault injection locations.

6. References

1. W. Yang, et al. Single-event-effect propagation investigation on nanoscale system on chip by applying heavy-ion microbeam and event tree analysis. Nuclear Science and Techniques, 2021(32):106