POLITECNICO DI TORINO

Dipartimento di Automatica e Informatica

PhD in Computer and Control Engineering

XXXI cycle

Supervisor

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Digital Design Techniques for Dependable High Performance Computing

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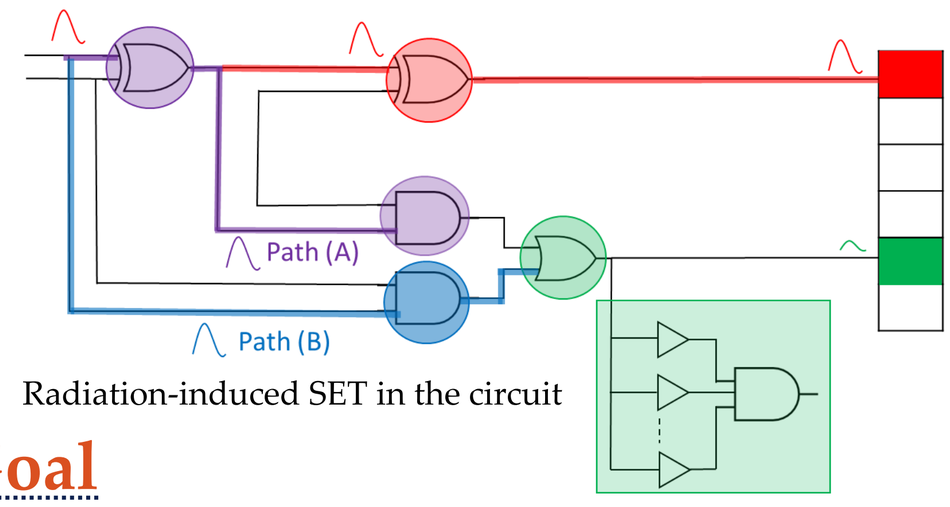
1. Introduction

Due to the decreasing of feature sizes of VLSI circuits, radiation induced Single Event Transients (SETs) are dominating the event ratio on modern devices. SETs can propagate through the circuit and be sampled by the storage element, leads to an error.



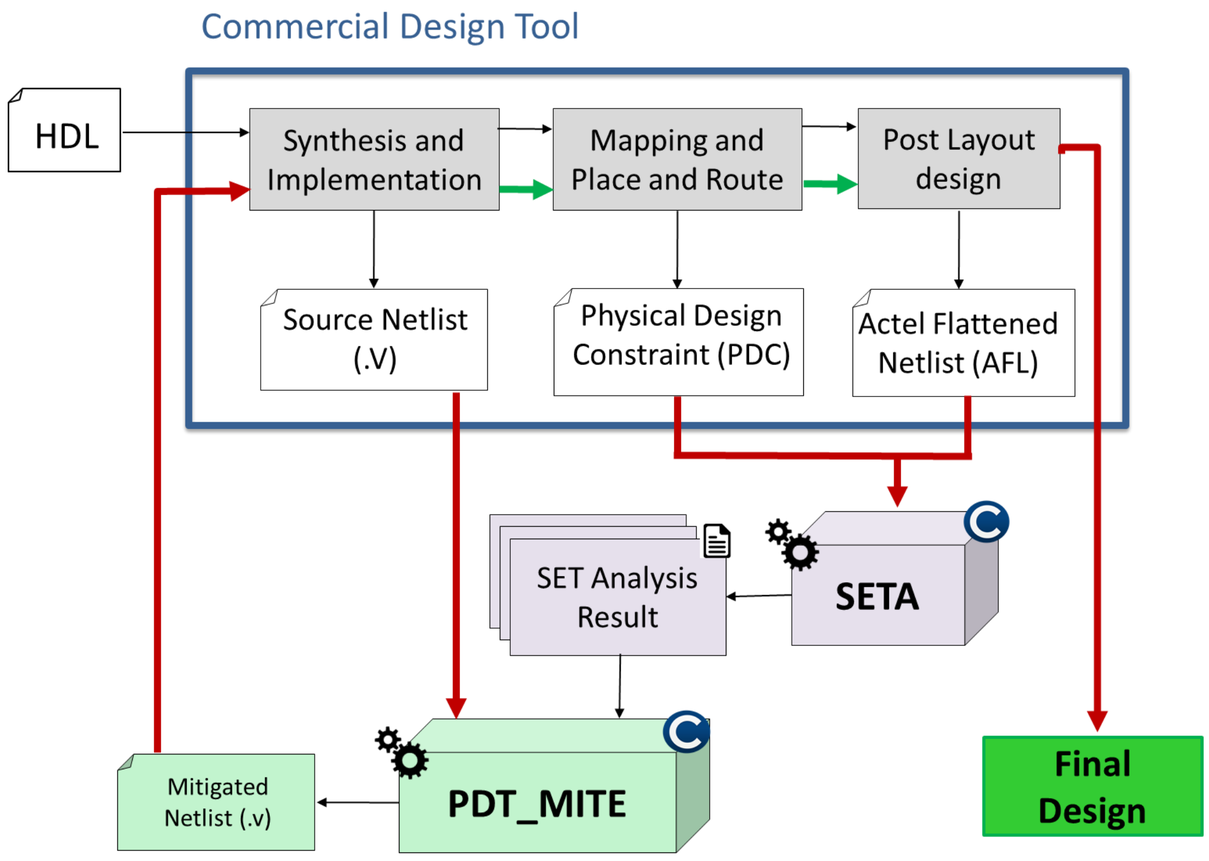
Radiation-induced SET in the circuit

2. Goal

The goal of this research is to propose a complete implementation flow including SET sensitivity analysis and effective fault tolerance of the circuits oriented to **aerospace** and **autonomous vehicle**.

3. Developed Workflow

The developed workflow includes a SET analyzer and netlist modifier for mitigating the circuit against SET.



The developed flow for the accurate evaluation and mitigation of SET effect.

- **SET Analysis**

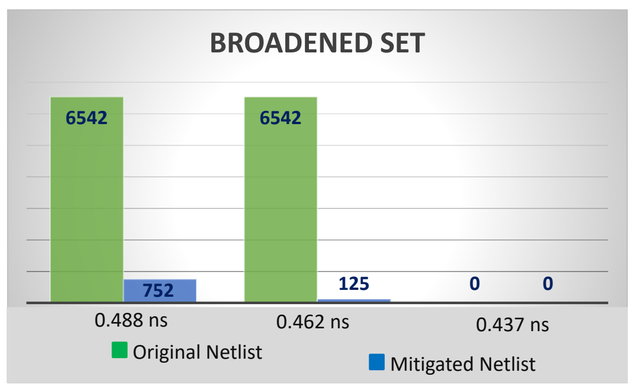
The first phase is providing an effective methodology for analysis of the SET sensitivity taking into account different SET propagation scenarios.

- **Mitigation Insertion**

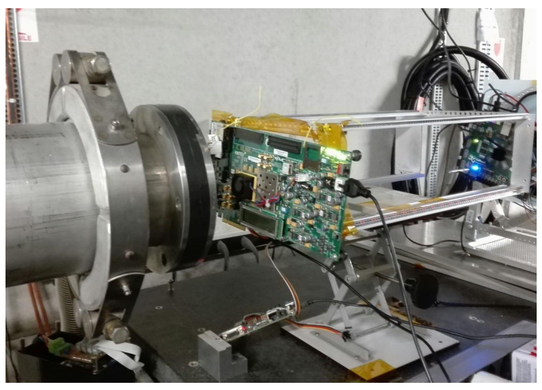
The circuit netlist is modified by inserting the filtering circuitry for SET mitigation. The tool modifies the plain netlist by adding filtering logics based on the performed SET analysis.

4. Results

This workflow has been applied to SoC embedded in **EUCLID European Space Agency** mission. Microsemi ProASIC3 Flash-based FPGA device has been used for implementing EUCLID circuit. For radiation exposure of 4Krad, SET pulses with duration between 0.43 ns and 0.48 ns have been considered.



SET Distribution Comparison Between Original Netlist and Mitigated Netlist



Heavy High Energy Heavy Ion Test Beam at CERN

5. References

1. **Azimi. S**, Du. B, Sterpone. L, Codinachs. D, Cattaneo. L, "*SETA: A CAD Tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs*", 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Application to Circuit Design (SMACD), July 2018.

2. **Azimi. S**, Du. B, Sterpone. L, "*On the Mitigation of Single Event Transients on Flash-based FPGAs*", 23rd IEEE European Test Symposium (ETS), May 2018.

3. **Azimi. S**, Du. B, Sterpone. L, "*Evaluation of Transient Errors in GPGPUs for Safety Critical Application: An Effective Simulation-based Fault Injection Environment*", Journal of Systems Architecture, - ISSN 1383-7621, April 2017.