

# Energy-Efficient Approximate Computing

PhD Candidate:

*Daniele Jahier Pagliari*

## 1. Introduction

Performance requirements in embedded systems are increasing, as emerging applications for the Internet of Things (IoT) require “intelligent” end-nodes. However, embedded devices are normally powered with batteries, and operate with very low energy budgets. Fortunately, many applications (machine learning, multimedia, etc.) exhibit some form of *error tolerance*, i.e. can accept a degradation in the quality of computations, without a significant impact on the quality of results. Error tolerance can be due to a number of different reasons, as shown in Figure 1.

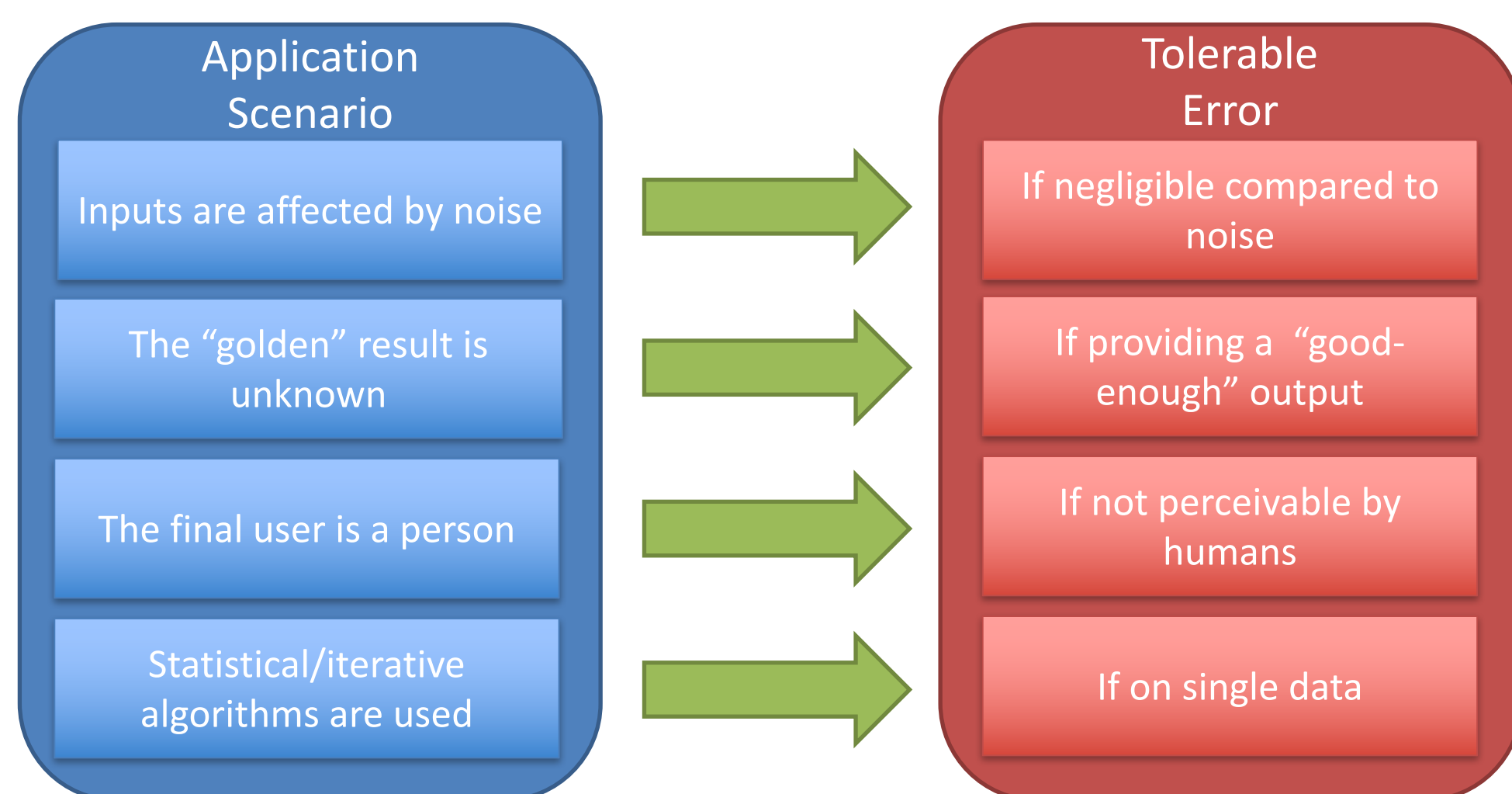


Figure 1. Error tolerance mechanisms.

Error tolerance can be exploited for energy efficiency, in what is called the **Approximate Computing (AC)** paradigm.

## 2. System-Level, Automated AC

The goal of this work is to develop new AC techniques that focus on *automation* and *generality*, and that consider **all components** of an embedded system, since the processor is not always the most energy-hungry element [3]-[5]. In particular, in the last three years, we worked on:

- **Hardware (HW) operators** (adders, multipliers) and **accelerators** (FIR, CORDIC, NPUs, etc.)
- **Serial interconnections**, both on-chip (e.g. NoC) and off-chip (e.g. sensor to processor).
- **OLED Displays**

## 3. Reconfigurable-Quality HW

We have proposed two different methods to design digital HW operators able to modify their computational quality at runtime. Both methods save energy by applying **supply voltage ( $V_{DD}$ ) scaling** beyond the limits imposed by classic design constraints.

In the first solution [1], the circuit is allowed to have **timing errors** due to the reduced  $V_{DD}$ , and the impact of these errors is *reduced* (but not eliminated) by an additional error-control circuit. In the second method [2], the operator **bit-width** is reduced to let it operate at low  $V_{DD}$  without violations, and **back-biasing** is applied at fine-grain, to improve the energy versus accuracy tradeoff.

Both methods can be applied **automatically**, to any **datapath operator**, regardless of architectural details.

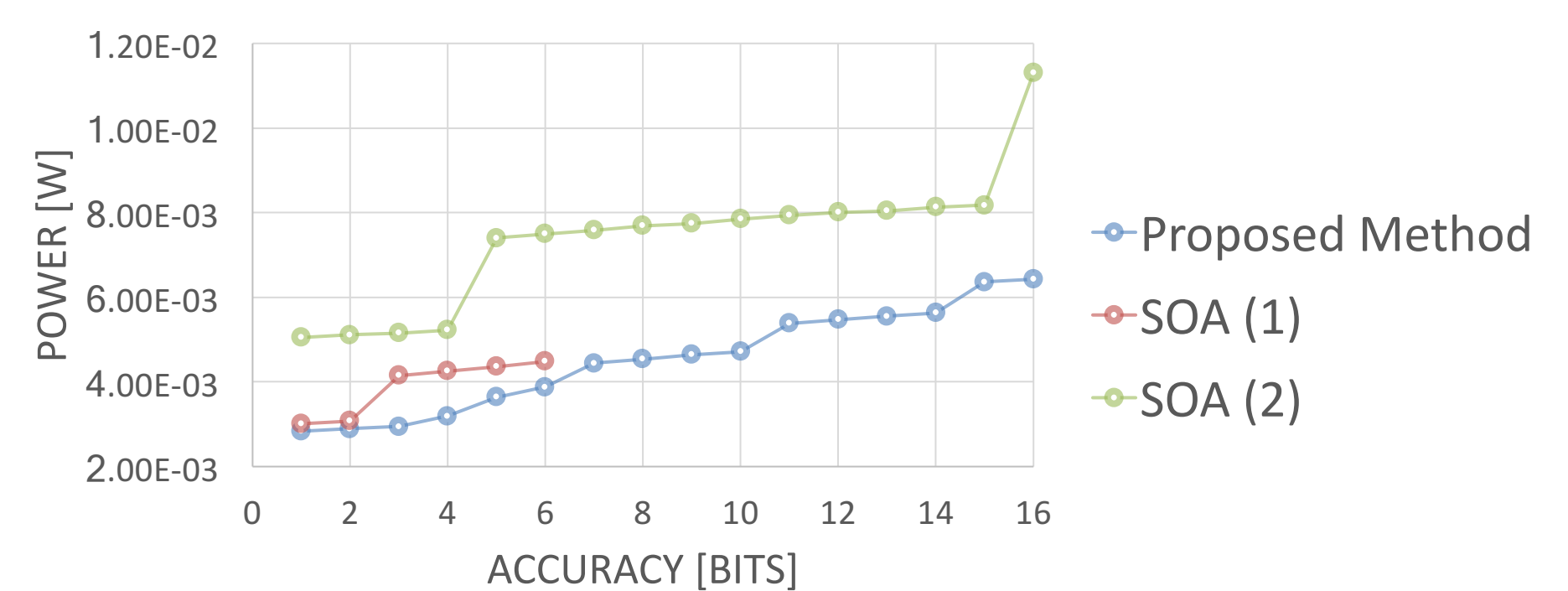


Figure 2. Power versus bit-width tradeoff for the method in [2] compared to the State-Of-the-Art (SOA)

## 4. Approximate Bus Encodings

To reduce energy consumption in serial interconnects, we have proposed two approximate bus encodings called **ADE** [3] and **Serial T0** [4]. The former is effective for generic (error tolerant data), while the latter specifically targets **temporally correlated data**, such as that produced when transmitting images.

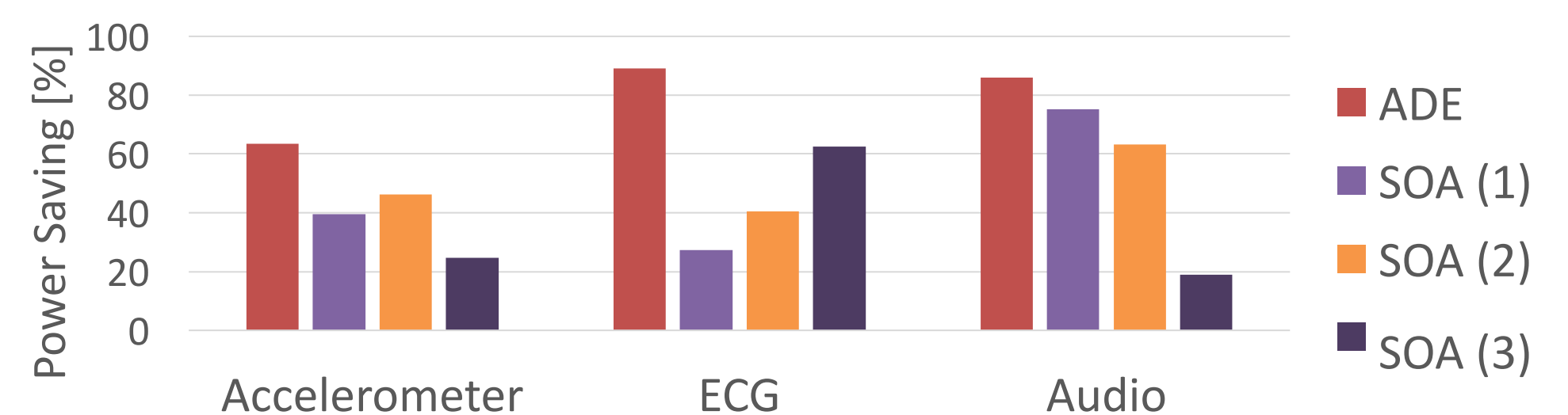


Figure 3. Saving in ADE [3] and SOA methods for different inputs, when a maximum error of 2% of the full-scale value is allowed.

## 5. Approximation in Displays

Differently from LCDs, the power in OLEDs strongly **depends on image pixels**. Therefore, energy can be reduced transforming (i.e. approximating) the displayed image. We have proposed a new transformation, called **LAPSE** [5], which focuses in particular on simplicity and **real-time applicability**. LAPSE achieves energy savings and quality comparable to the state of the art, despite a much **lower complexity**.

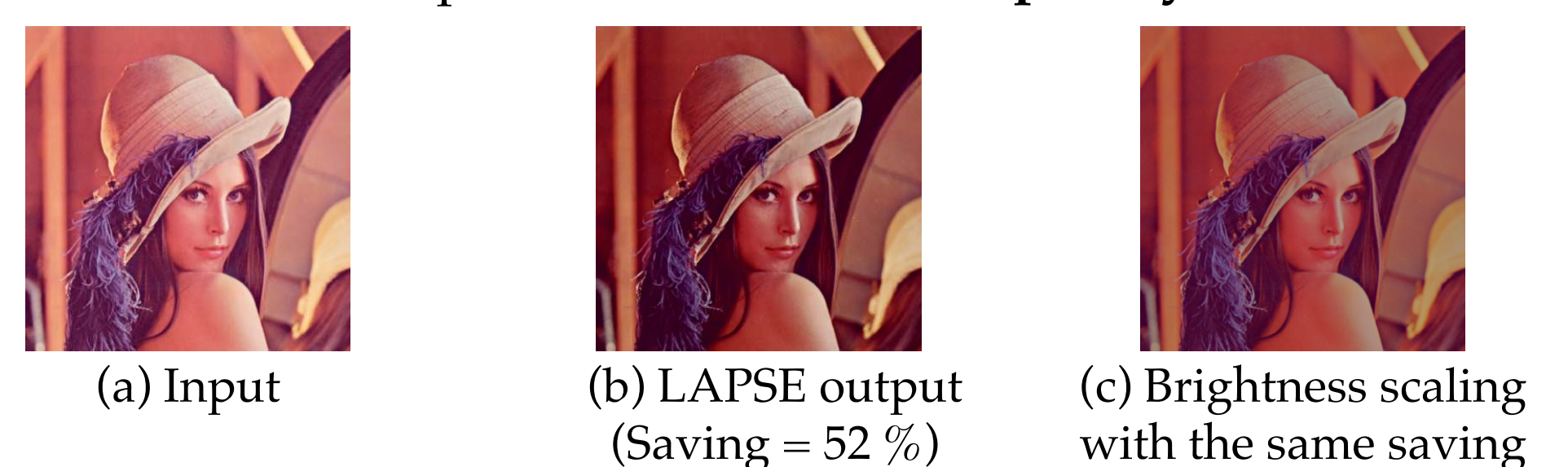


Figure 4. Example of image transformation with [5].

## 6. References

- [1] Jahier Pagliari et al.. “An automated design flow for approximate circuits based on reduced precision redundancy”. Proc. 33<sup>rd</sup> ICCD, 2015.
- [2] Jahier Pagliari et al. “A methodology for the design of dynamic accuracy operators by runtime back bias”. Proc. DATE 2017
- [3] Jahier Pagliari et al. “Approximate Energy-Efficient Encoding for Serial Interfaces”. ACM TODAES vol. 22 n. 4, 2017
- [4] Jahier Pagliari et al. “Zero-Transition Serial Encoding for Image Sensors”. IEEE Sensors Journal vol. 17, n. 8, 2017
- [5] Jahier Pagliari et al. “Low-overhead adaptive contrast enhancement and power reduction for OLEDs”. Proc. DATE, 2016