POLITECNICO DI TORINO
Dipartimento di Automatica e Informatica

PhD in Computer and Control Engineering

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Simulation of Non-functional Properties in Cyber-Physical Systems

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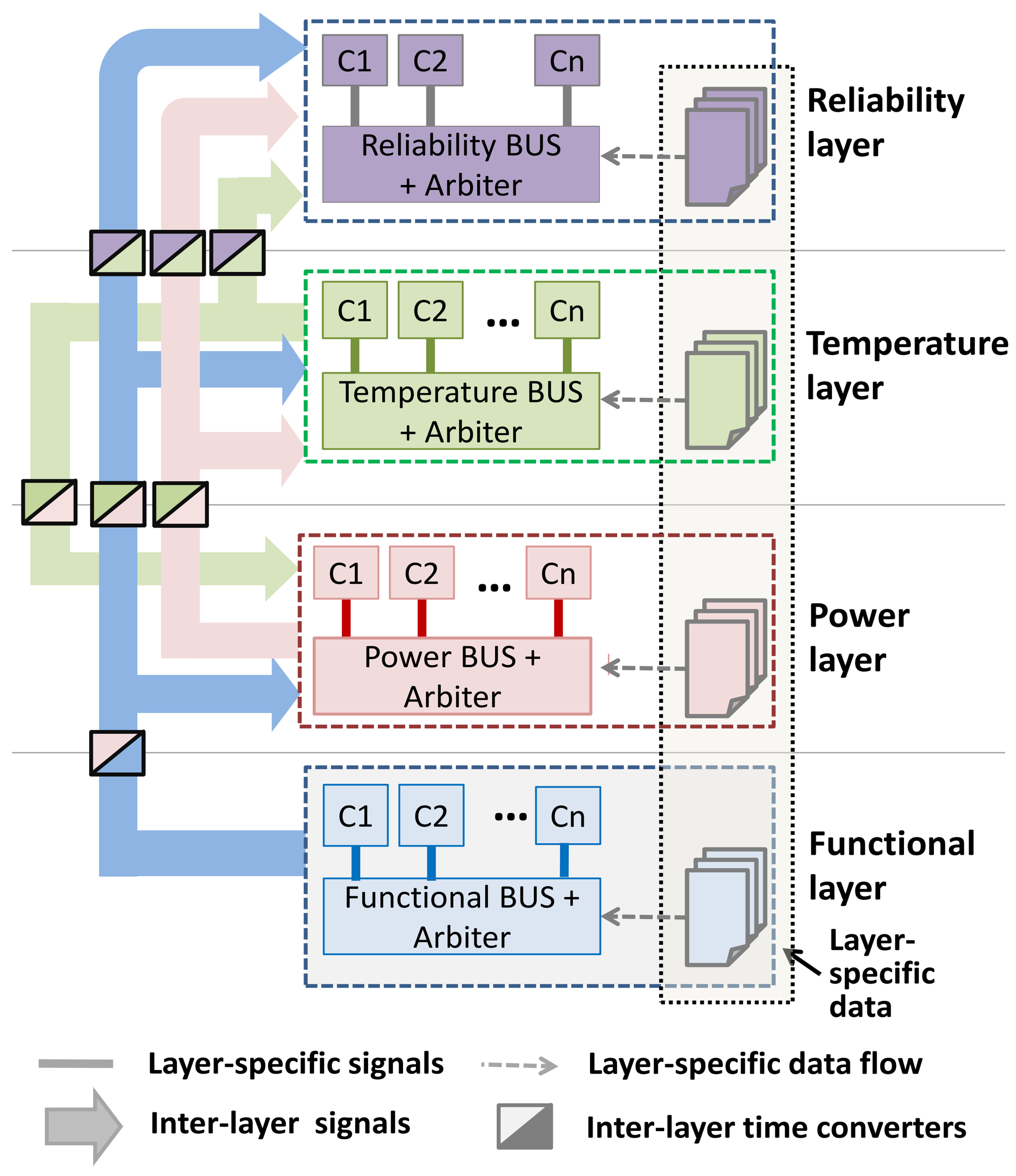
1. Introduction and Goal

Cyber Physical Systems (CPS) cover a wide variety of domains, ranging from analog to digital, together with power devices, sensors, actuators. This kind of heterogeneity has a heavy impact on their design process, as challenges are not restricted to functionality but rather related to a number of extra-functional properties, including power consumption, temperature and aging. The extra-functional properties need to be modeled and analyzed at the system level, because they can strongly affect the overall quality of service or even cause the system to fail meeting its real-time and safety requirements.

The goal of the research topic is to develop a novel simulation framework can simultaneously simulate functionality and non-functional properties of cyber-physical systems, also can conduct concurrent simulation with different non-functional properties of cyber-physical systems in order to reflect mutual effect of these extra-functional properties [1].

2. Proposed Simulation Framework

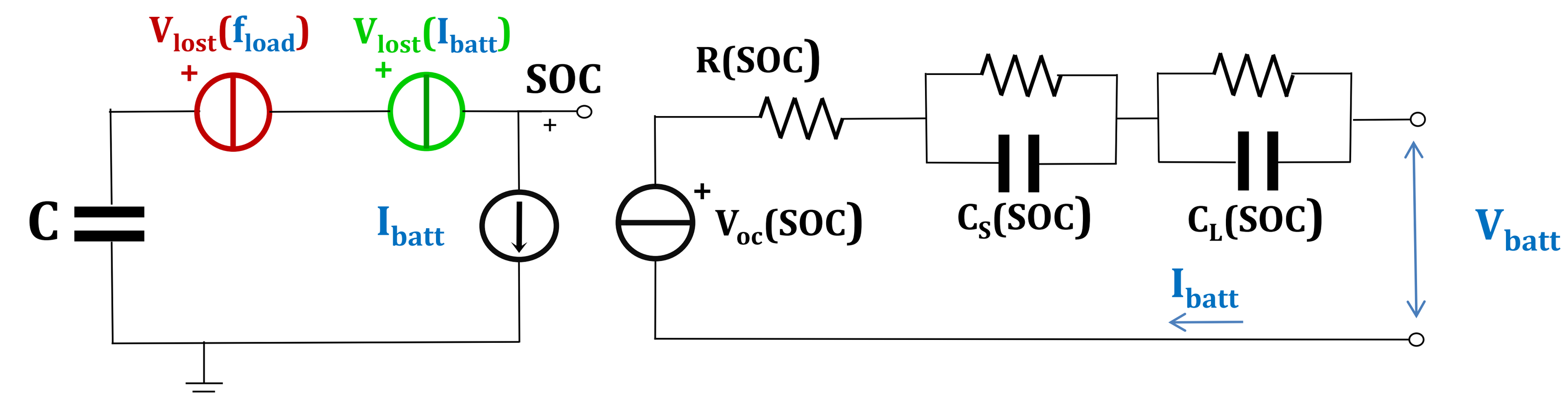


- ***Multi-Layered Structure*** : The reconciliation of both functional and extra-functional aspects to a single simulation infrastructure and language is achieved by structuring simulated system according to different views, called layers, each one relative to one specific property.
- ***Bus-Centric Modular Architecture*** : Each property is simulated by adopting a specific "virtual bus," which conveys and elaborates property-specific information, used to derive property-specific status of the overall system. This allows reducing all layers to a common flat structure, easing synchronization and information exchange.
- ***Different Time Scales*** : Each layer evolves according to its own "time constant," representing a realistic rate of update of the corresponding property. Each layer receives information from other layers after a conversion into the appropriate time scale for synchronization.
- ***Design Automation*** : Using standard functional description languages (IP-XACT, SystemC) to build automatically each layer structure and assemble different property-specific models in each layer, then complete overall simulation framework.

3. Accomplishment in Different Layers

- **Power Layer – Battery models**

State-of-the-art circuit equivalent battery models are only sensitive to the average current of load, but the load frequency and transient current value also affect battery performance. We added two voltage generators in state-of-the-art model to represent capacity dependence on instantaneous current value and load frequency [2]. In this way, we can conduct design exploration in the frequency domain to overcome the limitations of traditional methodology in time domain.

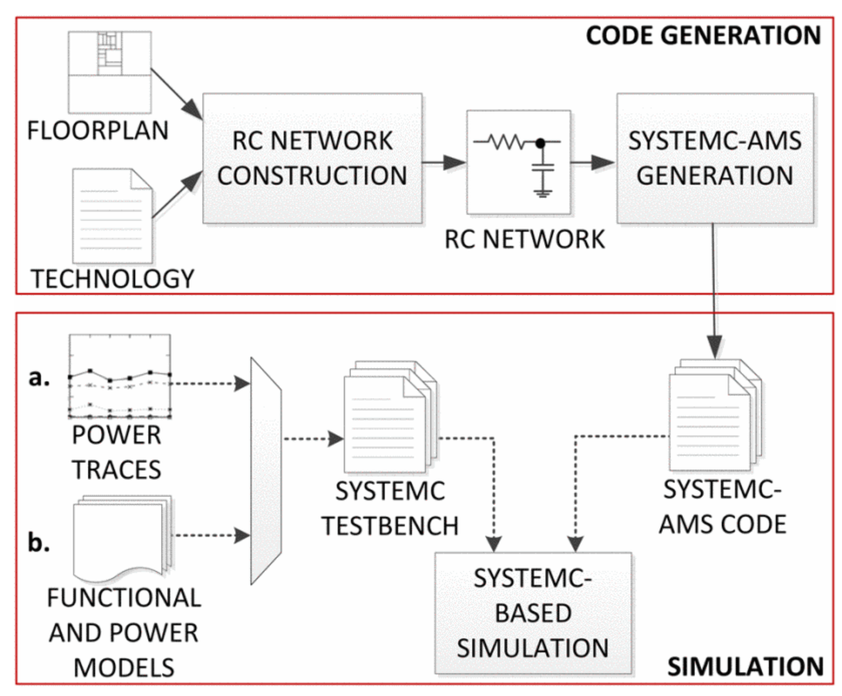


- **Temperature Layer – Thermal simulation**

Temperature is a critical property of smart systems, due to its impact on reliability and its inter-dependence with power consumption. Unfortunately, current design flows evaluate thermal evolution on offline power traces. This does not allow to consider temperature as a dimension in the design loop, and it misses all the complex inter-dependencies.

Proposed Thermal Simulator [3]

- ☐ Circuit-equivalent model
- ☐ Architecture simulation
- ☐ Different spatial granularities
- ☐ Steady state and transient trace
- ☐ Concurrent simulation
- ☐ High accuracy w.r.t *Hotspot*
- ☐ Fast simulation speed



- **Reliability Layer – NBTI aging model**

Since the long simulation time with traditional transistor-level NBTI aging model, we proposed a practical system-level NBTI aging macro-model for embedded microprocessor, where aging is expressed as a degradation of the maximum working frequency.

$$\hat{F}(t) = \boldsymbol{A} \cdot (\boldsymbol{W}, \boldsymbol{K}(V_{dd}, V_{th}, T, \mathrm{R}))$$

Because NBTI aging of the core is independent of the workloads (***W***), we can derived a fixed aging factor (***A***) to be interpreted as an equivalent signal probability to be used in a traditional transistor-level aging model. Characterization on different architectures and with different synthesis constraints (***K***) allows to yield lower and upper bounds for aging factor, best-case and worst-case aging scenarios can be inferred based on aging factor range [4].

4. References

1. Vinco, S., Chen, Y., Fummi, F., Macii, E. and Poncino, M., 2017. "A Layered Methodology for the Simulation of Extra-Functional Properties in Smart Systems". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.
2. Chen, Y., Macii, E. and Poncino, M., 2017." A circuit-equivalent battery model accounting for the dependency on load frequency". *Design, Automation & Test in Europe Conference & Exhibition* .
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4. Chen, Y., Macii, E. and Poncino, M., 2017. "Empirical derivation of upper and lower bounds of NBTI aging for embedded cores". *Microelectronics Reliability*.