POLITECNICO DI TORINO

Dipartimento di Automatica e Informatica

PhD in Computer and Control Engineering

XXIX cycle

Advisor

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Æthereal NoC blocking analysis

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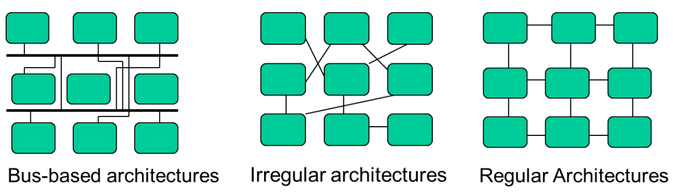
1. Networks on Chip?

"Network-on-a-chip (NoC) is a new paradigm for System-on-Chip (SoC) design. NoC based-systems accommodate multiple asynchronous clocking that many of today's complex SoC designs use. The NoC solution brings a networking method to on-chip communications and claims roughly a threefold performance increase over conventional bus systems."

2. Bus vs Networks-on-Chip (NoCs)



Bus-based architectures | Irregular architectures | Regular Architectures

Bus based interconnect

- Low cost
- Ease to Implement
- Flexibility

Networks on Chip

- Layered Approach
- Buses replaced with Networked architectures
  - Better electrical properties
  - Higher bandwidth
  - Energy efficiency
  - Scalability

3. Proposals

- Asynchronous NoCs
- Pure circuit switching

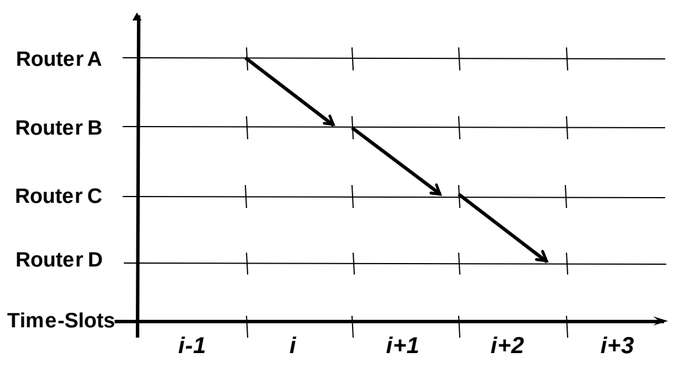
PHILIPS proposed to put the two worlds together

- Virtual circuit switching
  - share links (and buffers) in time (TDM) , e.g. Æthereal

4. Aethereal network on chip (The Synchronous thing)

- **multi-hop interconnect**
  - timing closure, GALS
  - modularity
- **guaranteed service (GS)**
  - real time
  - robustness
- **best-effort (BE)**
  - low cost
- **automated design flow**
  - dimensioning, incl. buffer sizing
  - performance closure

5. Æthereal operating principles



6. Forwarding Rules

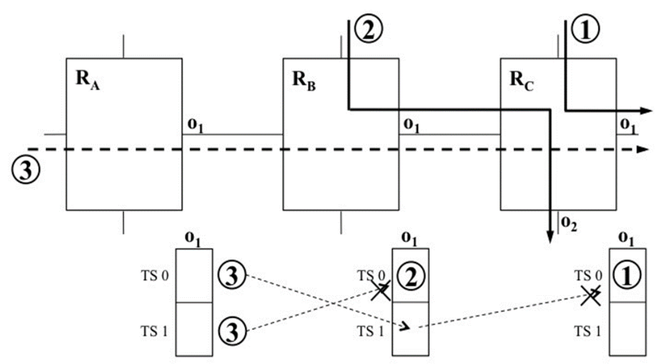
Rule 1. A packet p transmitted in time-slot t by router R_k must be transmitted in time-slot $(t + 1) \bmod S$ by router R_{k+1}.

Rule 2. A packet p transmitted in time-slot t by router R_k must be transmitted in time-slot $(t+d) \bmod S$, $d < S$ by router R_{k+1}.

7. BLOCKING ANALYSIS

- Unicast traffic, although multicast is supported in Æthereal.
- Poisson distributed GS connection arrivals.
- One time-slot per link capacity required by each connection.
- Random selection of time-slots at connection sources.
- Static routing, i.e., no alternative paths can be considered between each source/destination pair.
- Mutual independency of load distributions (i.e., distribution of reserved time-slots) at different links.

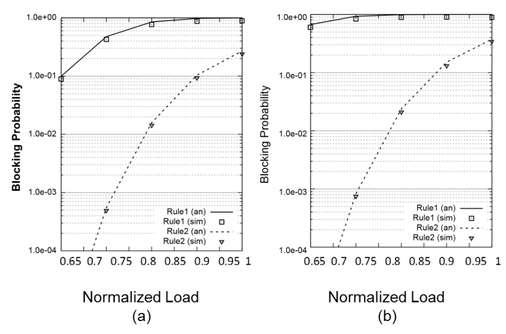
8. Un-schedulability in a simple Æthereal NoC



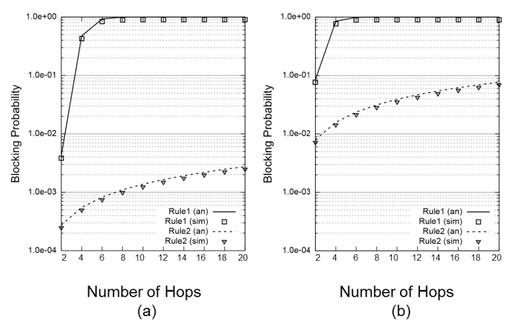
9. blocking probability at the last hop H:

$$P_b^{(H)} = P^{(H)}(S) = \sum_{i=0}^{S} \sum_{j=0}^{S} P(S|_{i,j})\, P^{(H-1)}{}_{(i)}\, P_{(j)}$$

10. Blocking Probability



Blocking probability as a function of the offered link load: (a) H =4; (b) H =6.

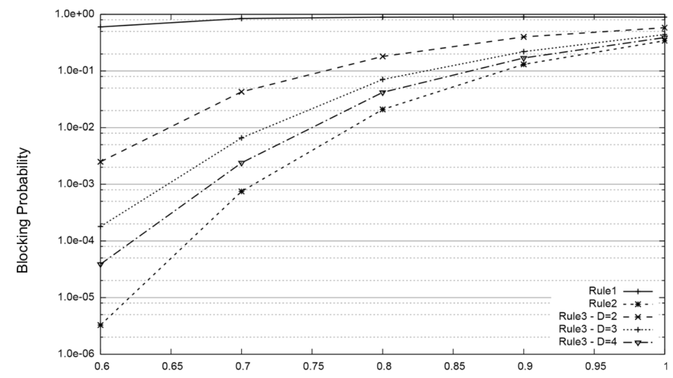


Blocking probability as a function of the path length: (a) ρ =0.7; (b) ρ =0.8

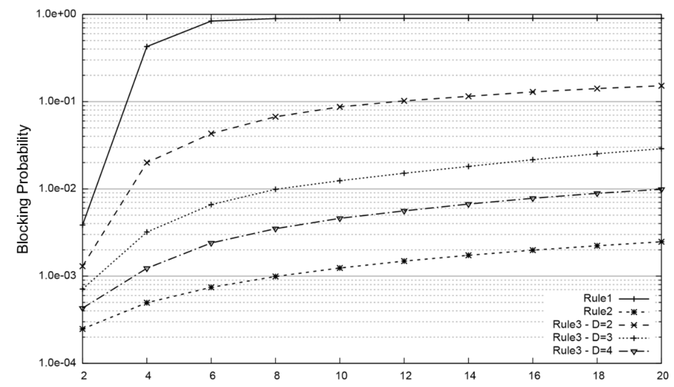
Æthereal NoC operating according to Rule 2 ensures a blocking probability lower than that obtained when Rule 1 is adopted. However, this operating mode is unfeasible due to its large buffering requirements.

11. Proposed Solution

Rule 3. A packet p transmitted in time-slot t by router R_k must be transmitted in time-slot $(t+d) \bmod S$, $d \leq D$ by router R_{k+1}.



Blocking probability for different operating modes as a function of the offered link load



Blocking probability for different operating modes as a function of the path length.

Small increments in buffer size result in a significant reduction of the blocking probability.

12. Conclusions

- Analytical model demonstrates how the blocking probability might be significant if resource reservation is performed at run-time and buffering is minimized
- Simulation shows how the blocking problem can be mitigated by means of small buffer size increments, thus defining a proper Æthereal operating rule that could satisfy both blocking (i.e., resource efficiency) and buffering constraints.

14. Publication

G. Marchetto, S. Tahir, M. Grosso "A Blocking Probability Study for the Aethereal Network-on-Chip", Submitted to IEEE International Design and Test Symposium (IDT 2016)

14. References

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[2]A. Hansson, M. Subburaman, and K. Goossens, "Aelite: A flit-synchronous Network on Chip with composable and predictable services," in Proc. of IEEE/ACM Design, Automation Test in Europe Conference Exhibition (DATE 2009)., 2009, pp. 250–255.

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