Æthereal NoC blocking analysis

1. Networks on Chip?
   “Network-on-a-chip (NoC) is a new paradigm for System-on-Chip (SoC) design. NoC based-systems accommodate multiple asynchronous clocking that many of today’s complex SoC designs use. The NoC solution brings a networking method to on-chip communications and claims roughly a threefold performance increase over conventional bus systems.”

2. Bus vs Networks-on-Chip (NoCs)
   ![Diagram showing different types of bus and network architecture]
   - **Bus-based architecture**
   - **Network-on-Chip (NoC)**
     - Low cost
     - Ease to Implement
     - Flexibility
     - Layered Approach
     - Buses replaced with Networked architectures
     - Better electrical properties
     - Higher bandwidth
     - Energy efficiency
     - Scalability

3. Proposals
   - Asynchronous NoCs
   - Pure circuit switching
   - PHILIPS proposed to put the two worlds together
     - Virtual circuit switching
       - share links (and buffers) in time (TDM), e.g. Æthereal

4. Æthereal network on chip (The Synchronous mode)
   - multi-hop interconnect
     - timing closure, GALS
   - guaranteed service (GS)
     - real time
   - best-effort (BE)
     - low cost
   - automated design flow
     - dimensioning, incl. buffer sizing
     - performance closure

5. Æthereal operating principles
   ![Diagram of network operation]

6. Forwarding Rules
   **Rule 1** A packet \( p \) transmitted in time-slot \( t \) by router \( R_i \) must be transmitted in time-slot \( (t+1) \mod S \) by router \( R_{i+1} \).
   **Rule 2** A packet \( p \) transmitted in time-slot \( t \) by router \( R_i \) must be transmitted in time-slot \((t+d) \mod S, d < S\) by router \( R_{i+d} \).

7. BLOCKING ANALYSIS
   - Unicast traffic, although multicast is supported in Æthereal.
   - Poisson distributed GS connection arrivals.
   - One time-slot per link capacity required by each connection.
   - Random selection of time-slots at connection sources.
   - Static routing, i.e., no alternative paths can be considered between each source/destination pair.
   - Mutual independency of load distributions (i.e., distribution of reserved time-slots) at different links.

8. Un-schedulability in a simple Æthereal NoC
   ![Diagram illustrating un-schedulability]

9. blocking probability at the last hop H:
   \[ P_b(H) = P(S) = \sum_{i=0}^{S} P(S_i) \cdot P^{i+1}(0) \cdot P(0) \]

10. Blocking Probability
    ![Blocking probability graph]

11. Proposed Solution
    **Rule 3** A packet \( p \) transmitted in time-slot \( t \) by router \( R_i \) must be transmitted in time-slot \((t+d) \mod S, d < S\) by router \( R_{i+d} \).

Small increments in buffer size result in a significant reduction of the blocking probability.

12. Conclusions
    - Analytical model demonstrates how the blocking probability might be significant if resource reservation is performed at run-time and buffering is minimized
    - Simulation shows how the blocking problem can be mitigated by means of small buffer size increments, thus defining a proper Æthereal operating rule that could satisfy both blocking (i.e., resource efficiency) and buffering constraints.

14. Publication
    G. Marchetto, S. Tahir, M. Grosso “A Blocking Probability Study for the Æthereal Network-on-Chip”, Submitted to IEEE International Design and Test Symposium (IDT 2016)

14. References

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